

ST-2 UMA LOGIC SCHEMATICS

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7.CPU(5/16) : RTC/HDA/SATA/JTAG

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20.BLANK

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24.DDR3L BASE MEMORY CH-A (1/2)

25.DDR3L BASE MEMORY CH-A (2/2)

26.DDR3L SO DIMM CHANNEL-B

27.BLANK

28.BLANK

29.BLANK

30.BLANK

31.BLANK

32.BLANK

33.BLANK

34.BLANK

35.BLANK
- 36.BLANK

37.BLANK

38.LCD CONNECTOR

39.BLANK

40.EXT CRT INTERFACE

41.DISPLAY PORT CONNECTOR

42.BLANK

43.SATA HDD CONN

44.BLANK

45.USB POWER/CONN

46.GBE CLARKVILLE

47.GBE LAN SWITCH

48.GBE MAGNETICS

49.RJ45 CONNECTOR

50.PCIE MINI CARD SLOT

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66.BLANK

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78.DC/DC VCC5M/VCC3M(TPS51220A)

79.DC/DC VCCCPUCORE(VT1328M)

80.DC/DC VCCCPUCORE(VT1334S)

81.BLANK

82.VCCCPUCORE DECOUPLING

83.BLANK

84.BLANK

85.DC/DC VCC1R05AMT(VT384B)

86.DC/DC VCC1R35A(VT387B)

87.DC/DC VCC0R675B(TPS51200)

88.BLANK

89.BLANK

90.BLANK

91.BLANK

92.DC/DC VCC1R5B(BU15TD2WNVX)

93.LOAD SW PCH SUS

94.LOAD SW LAN

95.BLANK

96.LOAD SW B

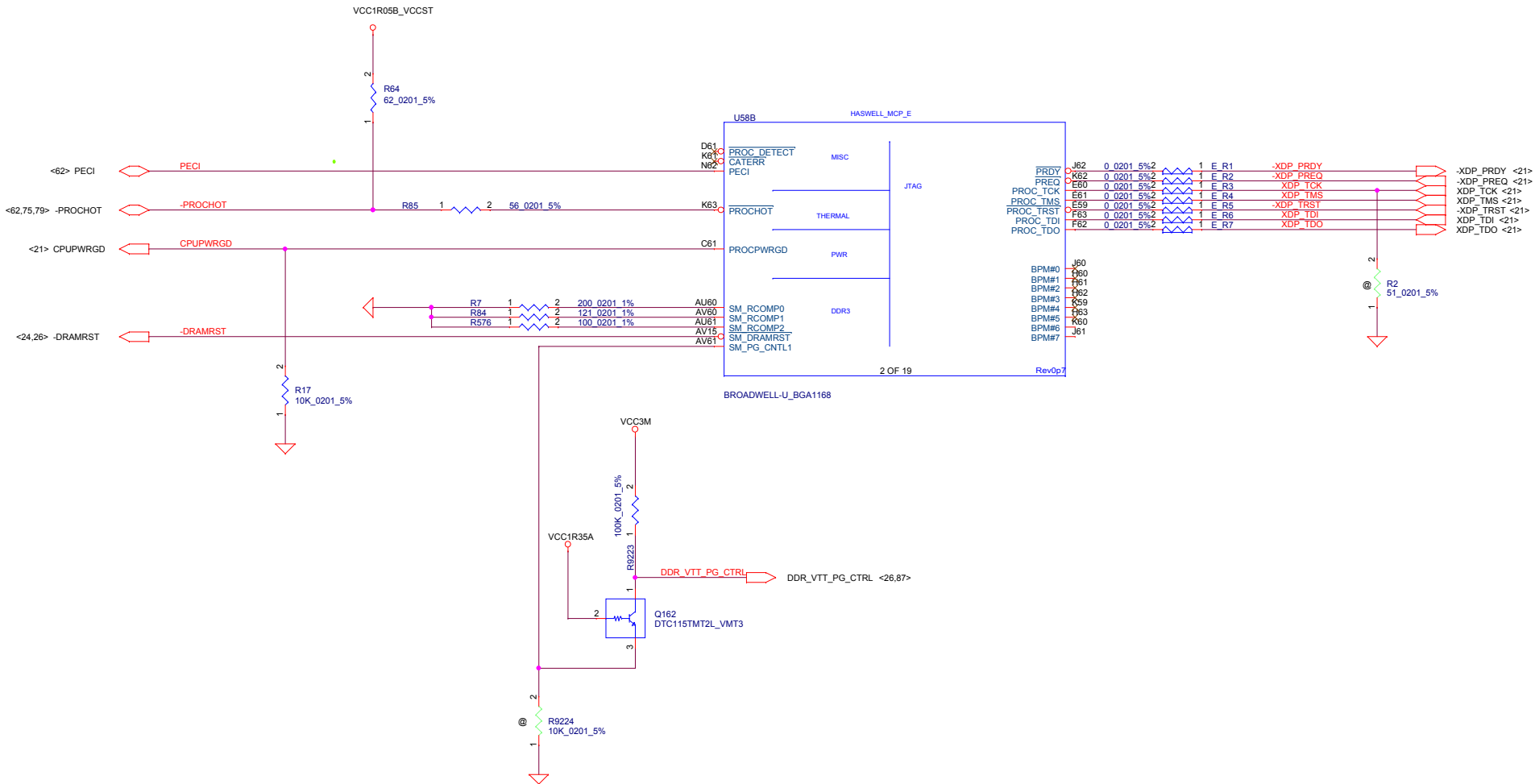
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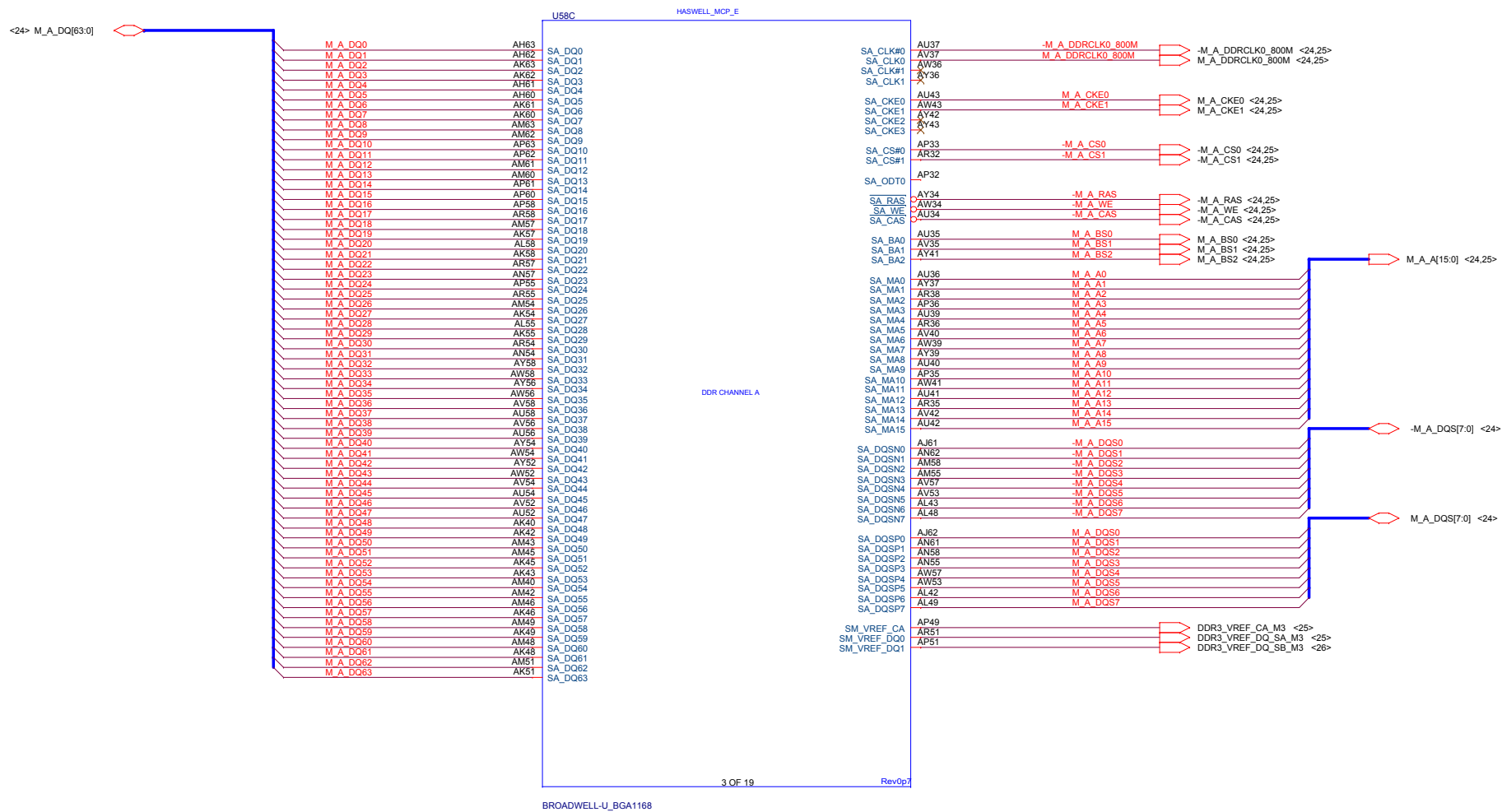
98.LOAD SW WWAN & WLAN

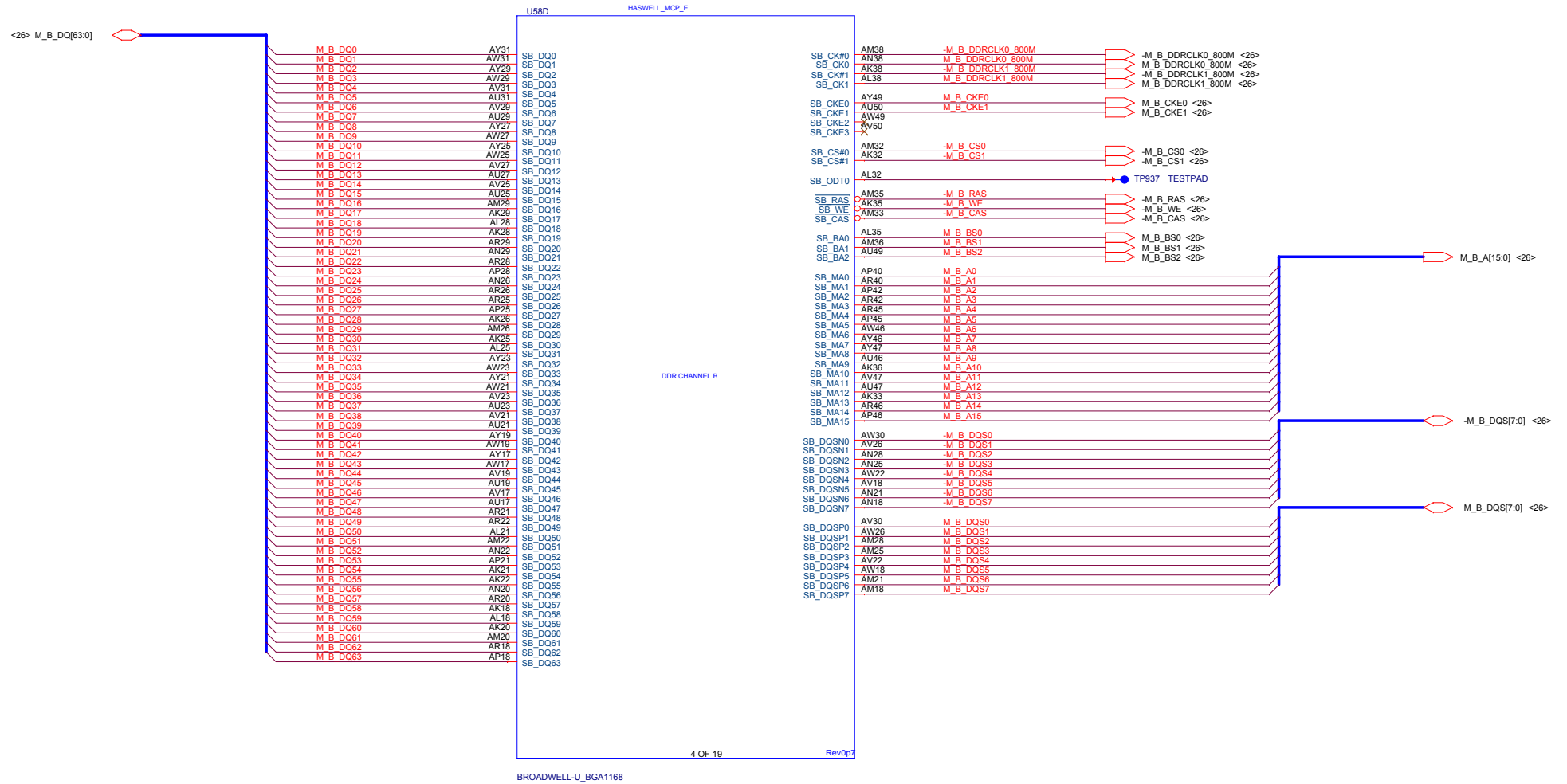
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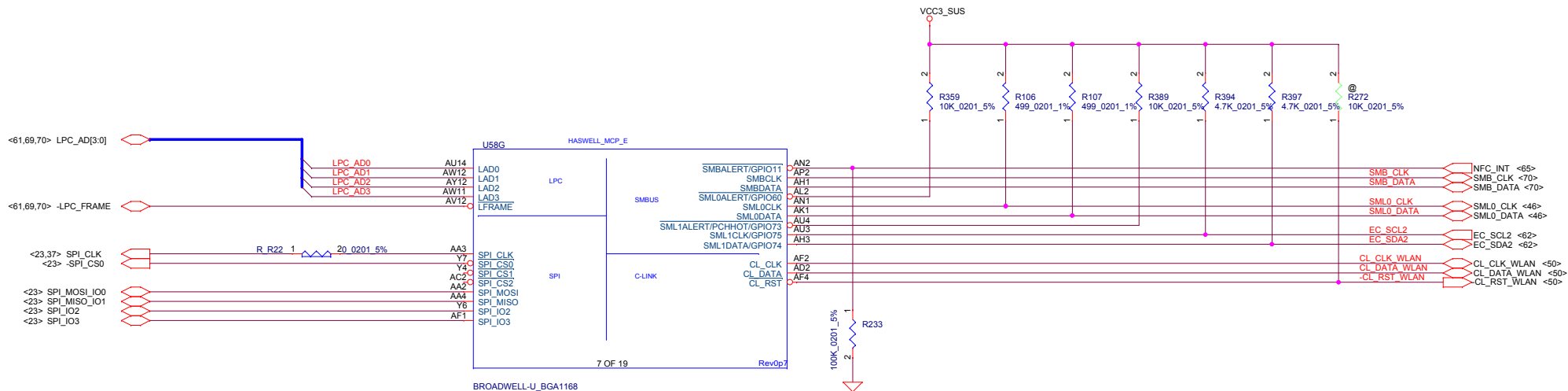
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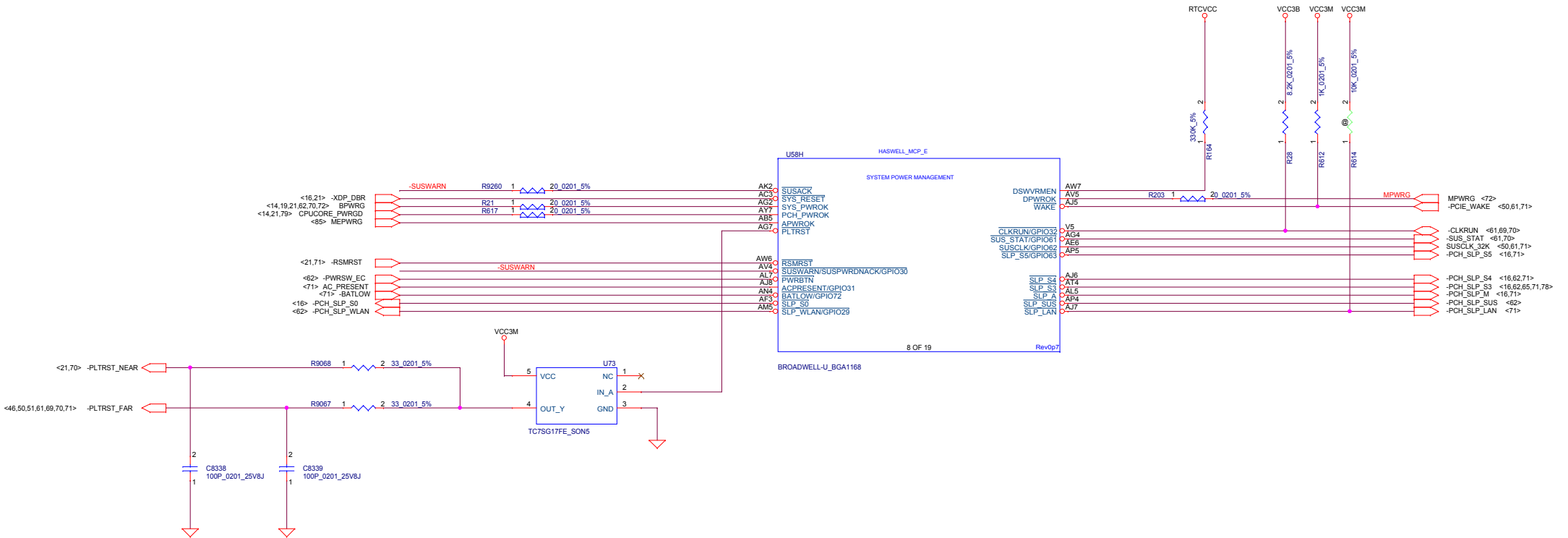
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2013/8/30	ST-2_UMA_SDV_EC007-010	JV_ST-2_UMA_SDV_SCH_EC007-010_083001.pdf
2013/9/5	ST-2_UMA_SDV_EC011	JV_ST-2_UMA_SDV_SCH_EC011_090501.pdf
2013/12/11	ST-2_UMA_SDV2_ECR001-002	JV_ST-2_UMA_SDV2_SCH_ECR001-002_121101.pdf








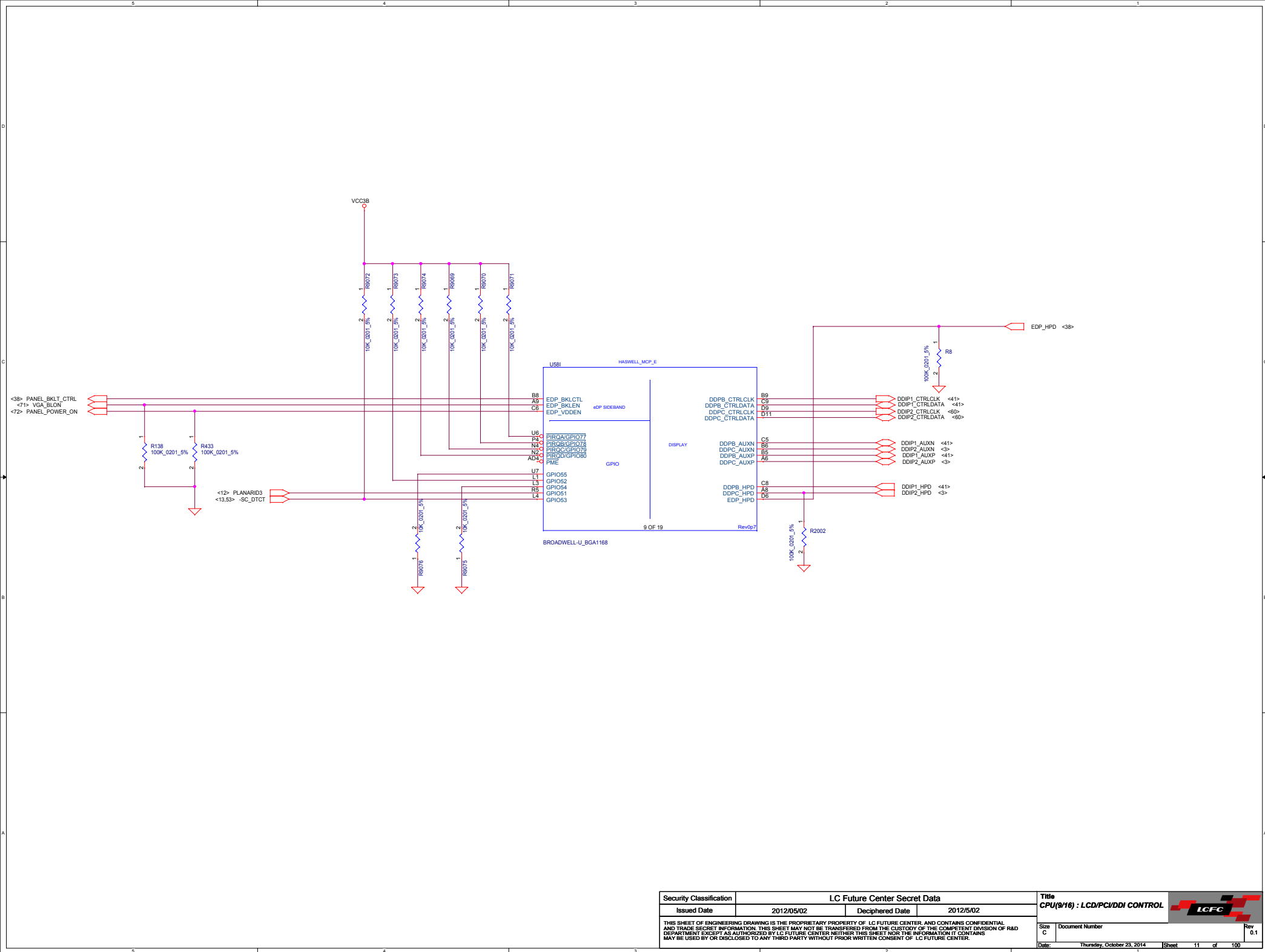


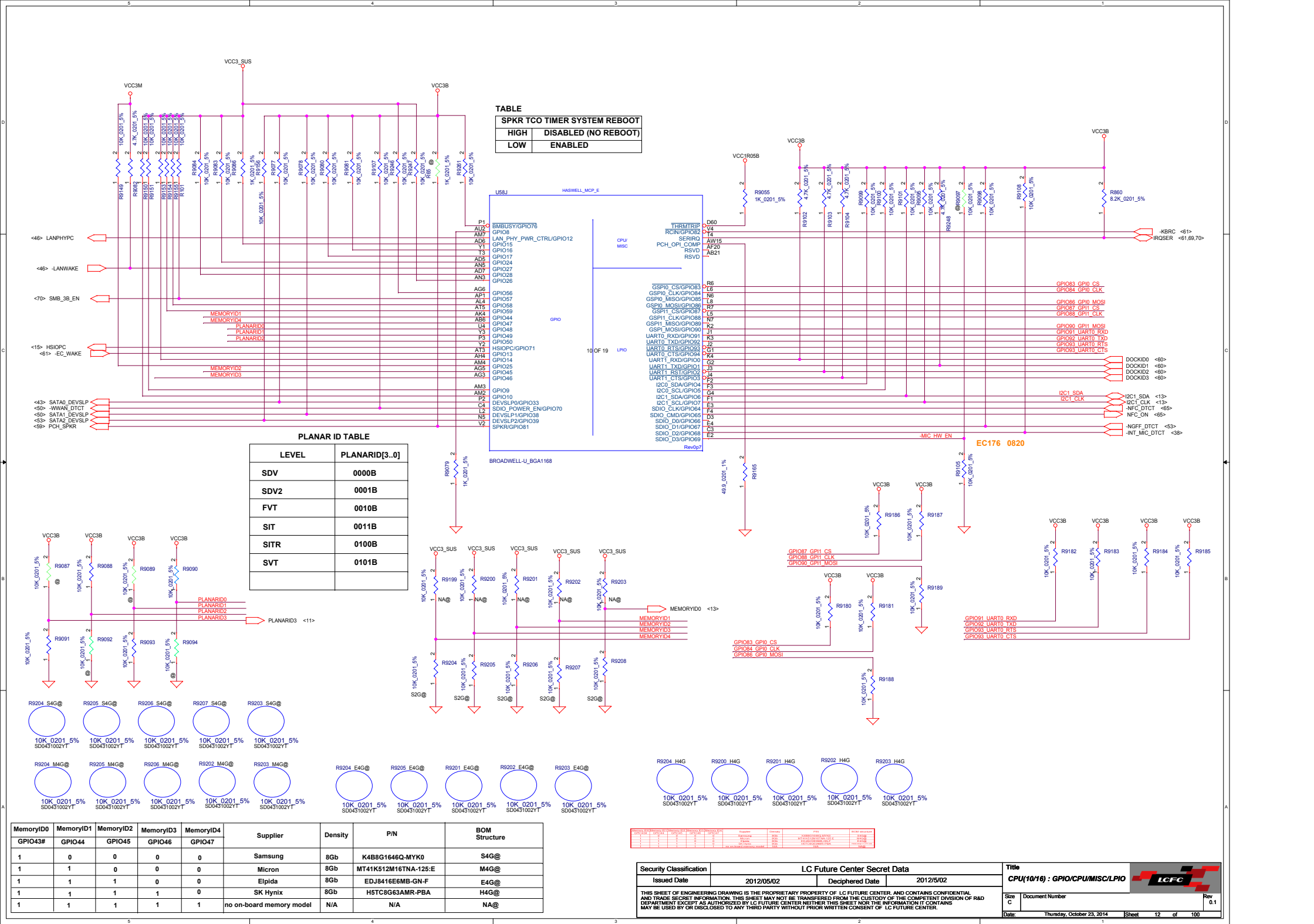


TABLE

CFG2 : PEG Static Lane Reversal 1 : Normal Operation 0 : Lane Reversal
CFG4 : Display Port Presence 1 : Disabled 0 : Enabled
CFG[6:5] : PEG Bifurcation 11 : Func 1 Disabled, Func 2 Disabled (x16,---,---) 10 : Func 1 Enabled, Func 2 Disabled (x8,x8,---) 01 : Func 1 Disabled, Func 2 Enabled 00 : Func 1 Enabled, Func 2 Enabled (x8,x4,x4)
CFG7 : PEG Defer Training 1 : PEG Train Immediately Following XXRESETB Deassertion 0 : PEG Wait for BIOS for Training

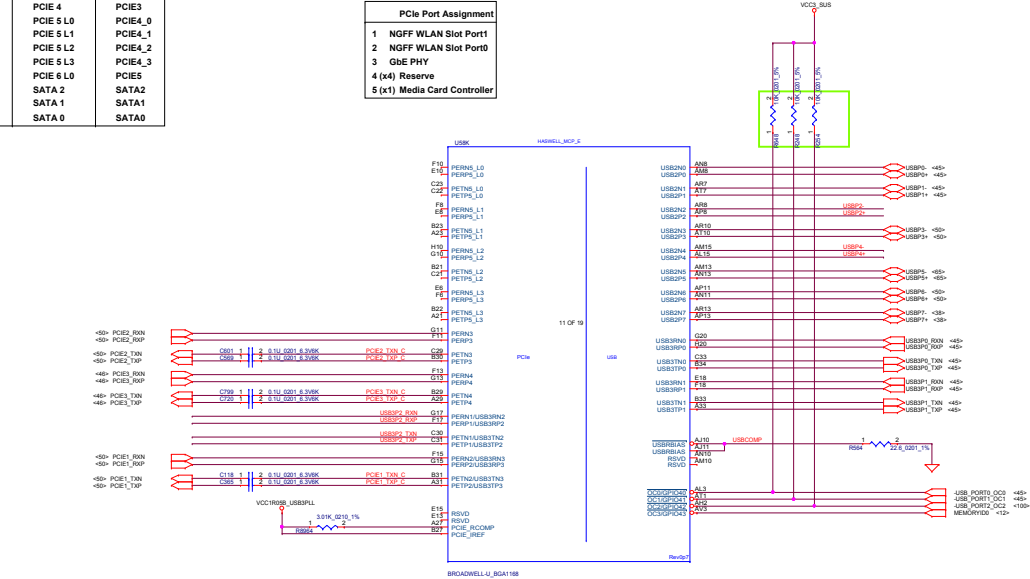
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								<p>STING UMA</p>								Date:		Thursday, October 23, 2014		Sheet 10 of 100	





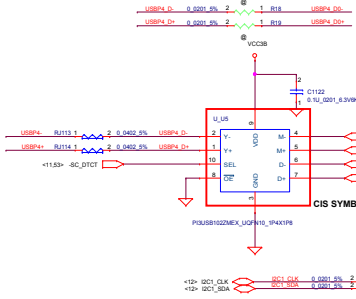
Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2	USB3 2	USB3P1
Port 3	PCIE 1/USB3 3	USB3 3	USB3P2
Port 4	PCIE 2/USB3 4	PCIE 1	PCIE1
Port 5	PCIE 3	PCIE 2	PCIE2
Port 6	PCIE 4	PCIE 3	PCIE3
Port 7	PCIE 5 L0	PCIE 5 L0	PCIE4_0
Port 8	PCIE 5 L1	PCIE 5 L1	PCIE4_1
Port 9	PCIE 5 L2	PCIE 5 L2	PCIE4_2
Port 10	PCIE 5 L3	PCIE 5 L3	PCIE4_3
Port 11	PCIE 6 L0	PCIE 6 L0	PCIE5
Port 12	SATA 2/PCIE 6 L1	SATA 2	SATA2
Port 13	SATA 1/PCIE 6 L2	SATA 1	SATA1
Port 14	SATA 0/PCIE 6 L3	SATA 0	SATA0

PCIE Port Assignment	
1	NGFF WLAN Slot Port1
2	NGFF WLAN Slot Port0
3	GbE PHY
4 (x4)	Reserve
5 (x1)	Media Card Controller



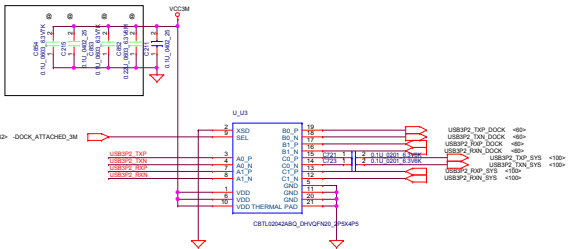
USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	USB 3.0 Docking/3rd USB3.0 System Port
3	NGFF WWAN Slot
4	Smart Card Slot / Touch Panel
5	Fingerprint Reader
6	NGFF WLAN Slot
7	USB Camera

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB 3.0 System Port (Debug)
2	USB 3.0 Docking/3rd USB3.0 System Port



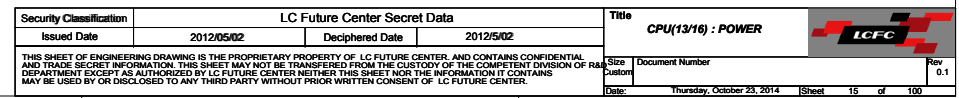
Device Selection	
0	Smart Card Slot
1	Touch Panel

PN Apply



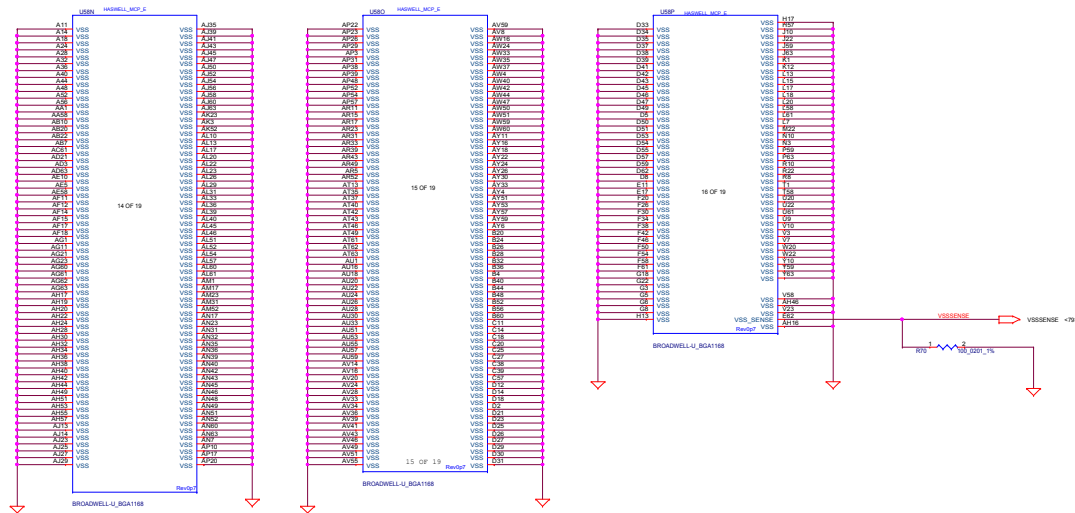
Vendor	P/N
Pericom	PI3PCIE3212
NXP	CBTL02043ABQ

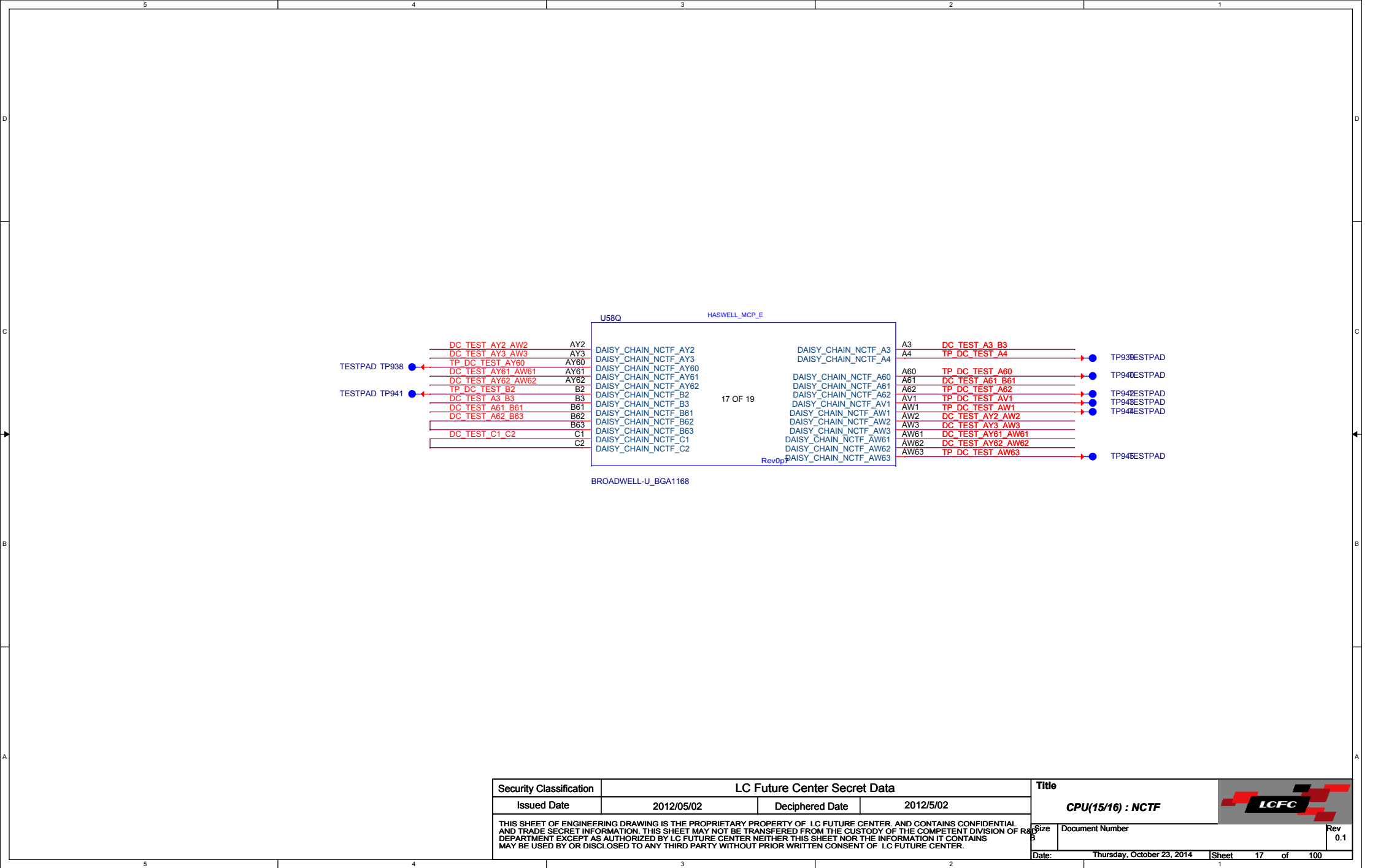
Vendor	P/N
Pericom	PI3USB1022ME
NXP	NX3DV42GU



Module Pin	Header Pin
1	VCC3_SBS
2	VCC3M
3	GND
4	SLP_S0M
5	GND1
6	SYS_RESET#
7	GND2
8	PWRSTNR
9	GND3
10	RTCRST#
11	GND4
12	+V3.3DS
13	SLP_A#
14	SLP_S#M
15	SLP_S#
16	VDDCRST3_3
17	SLP_S#M
18	VDDCRST3_3

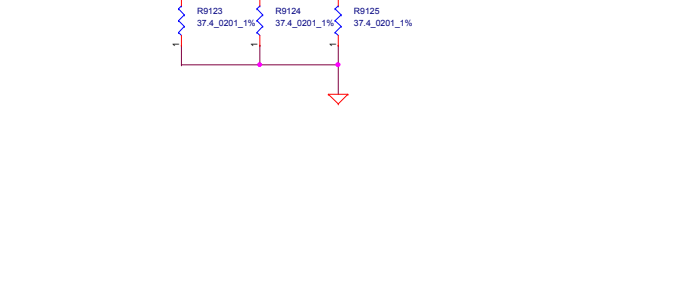
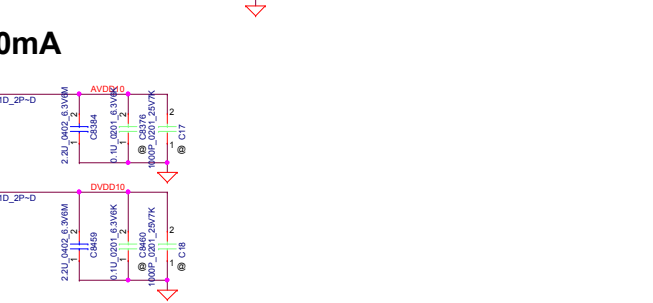
CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM







CFG4: Display Port Presence
1: Disabled 0: Enabled




[illegible]

Max 130mA

2.2uF, 0.1uF, 1000pF: Near filter

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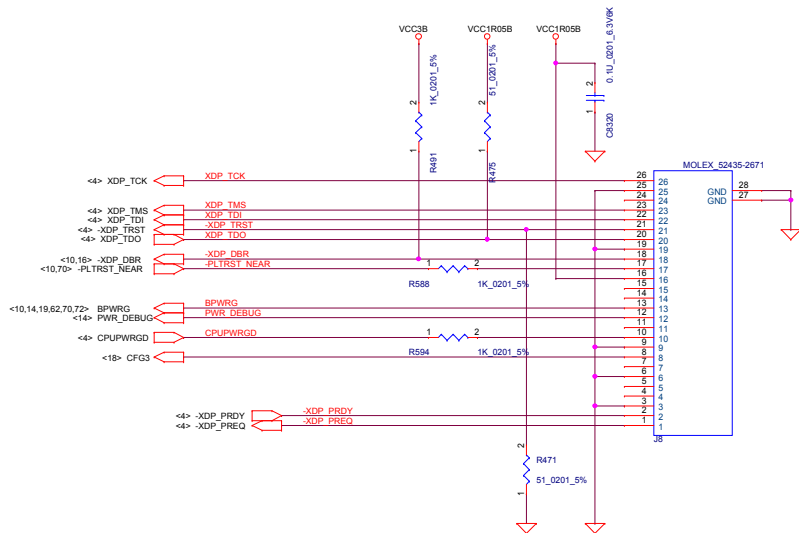


TABLE : CPU ITP DEBUG REPORT

SIGNAL	REF DES	Planar Only	BOX
TDO	R475	ASM	ASM
TRST#	R471	ASM	ASM
DBRST#	R491	ASM	ASM
RESET#	R588	ASM	ASM
PWRGD	R594	ASM	ASM
CONNECTOR	J8	ASM	NO ASM

NOTE : APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV

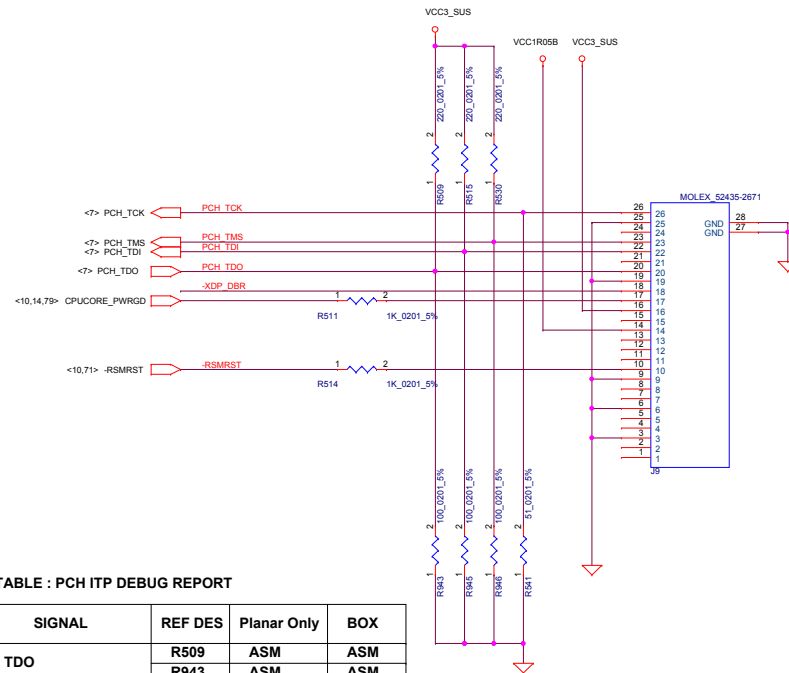
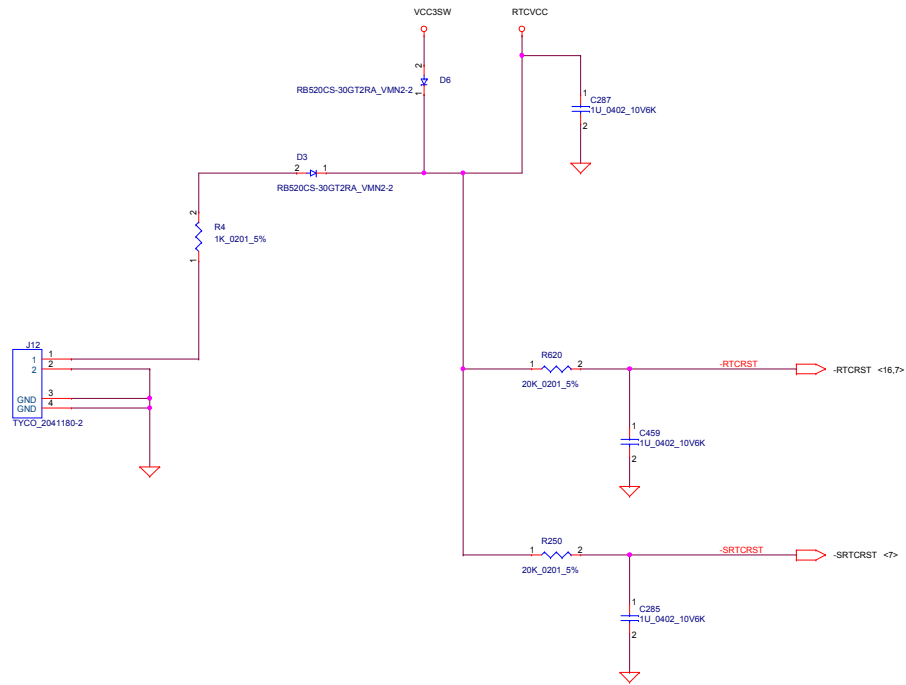




TABLE : PCH ITP DEBUG REPORT

SIGNAL	REF DES	Planar Only	BOX
TDO	R509	ASM	ASM
	R943	ASM	ASM
TMS	R530	ASM	ASM
	R946	ASM	ASM
TDI	R515	ASM	ASM
	R945	ASM	ASM
TCK	R541	ASM	ASM
CPUCORE_PWRGD	R511	ASM	ASM
-RSMRST	R514	ASM	ASM
CONNECTOR	J9	ASM	NO ASM

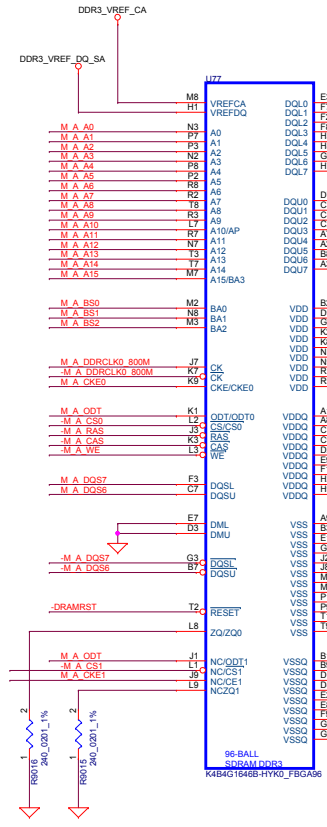
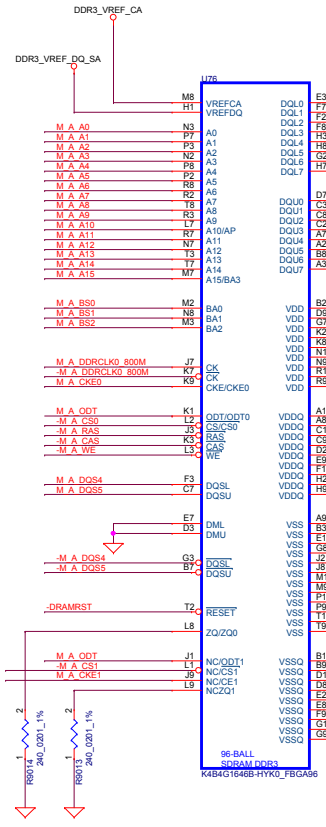
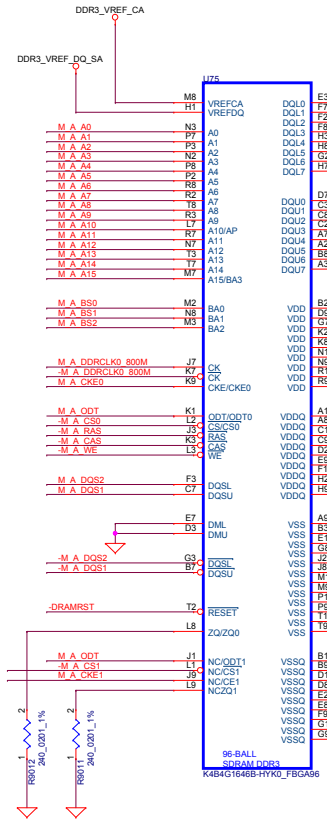
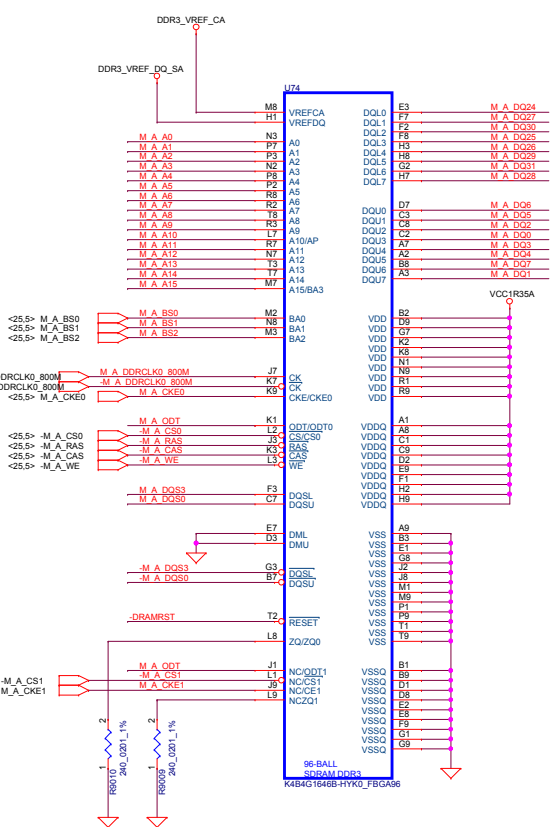
NOTE : APPLY EACH LOGIC ACCORDING TO CONFIGURATION IN SDV



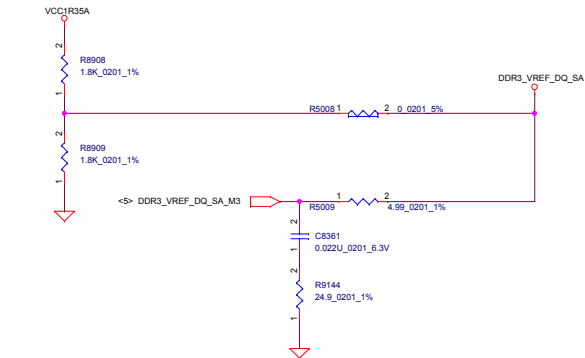
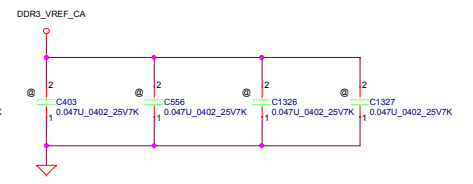
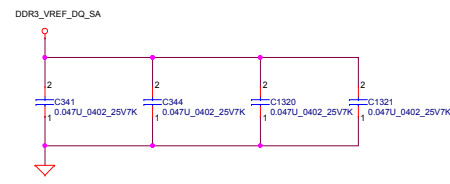
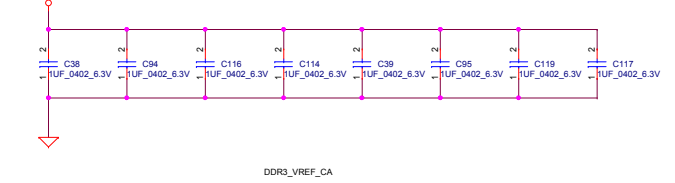
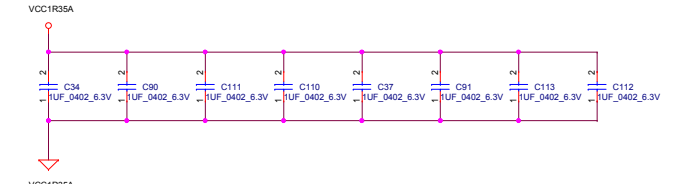
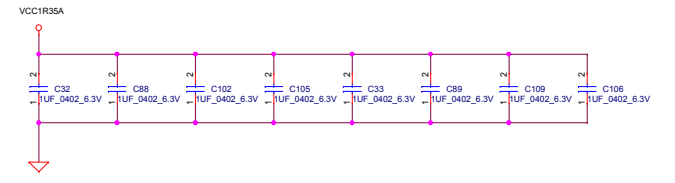
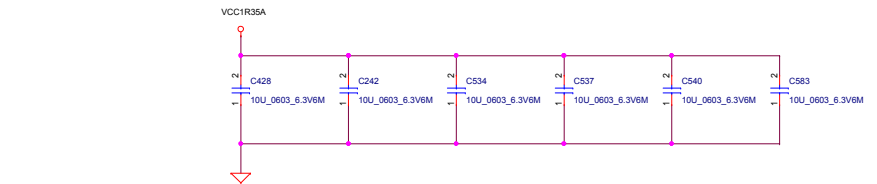
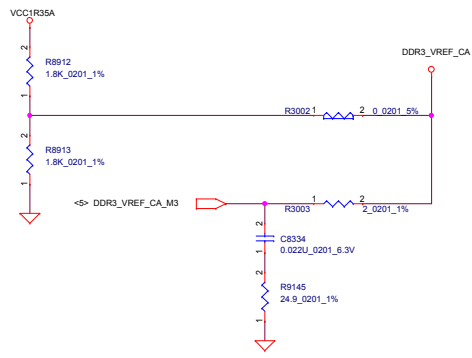
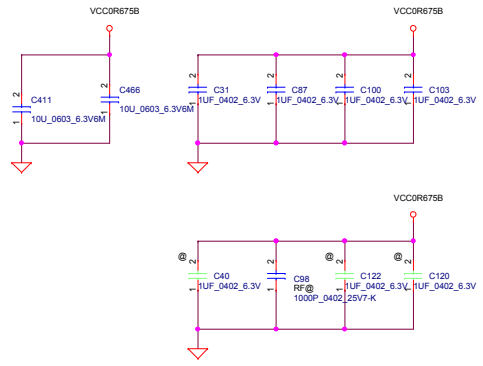
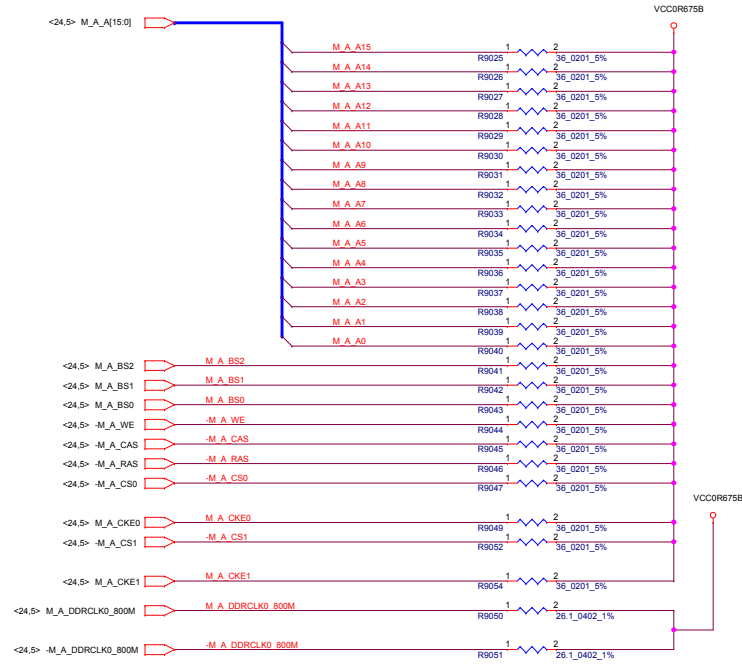
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<5> M_A_DQ[63:0]
<5> M_A_DQS[7:0]
<5> M_A_DQS[7:0]
<25.5> M_A_A[15:0]

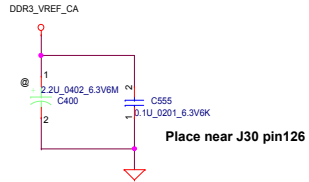


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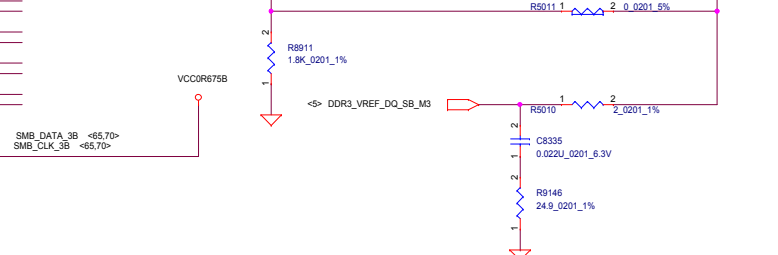
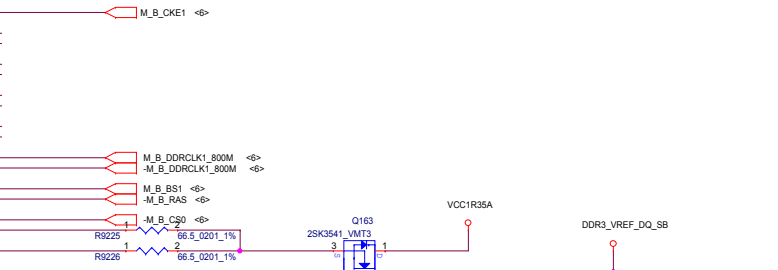
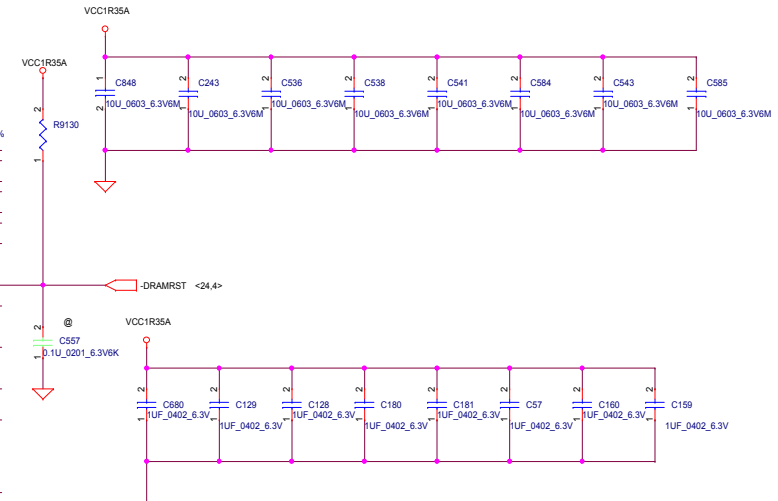
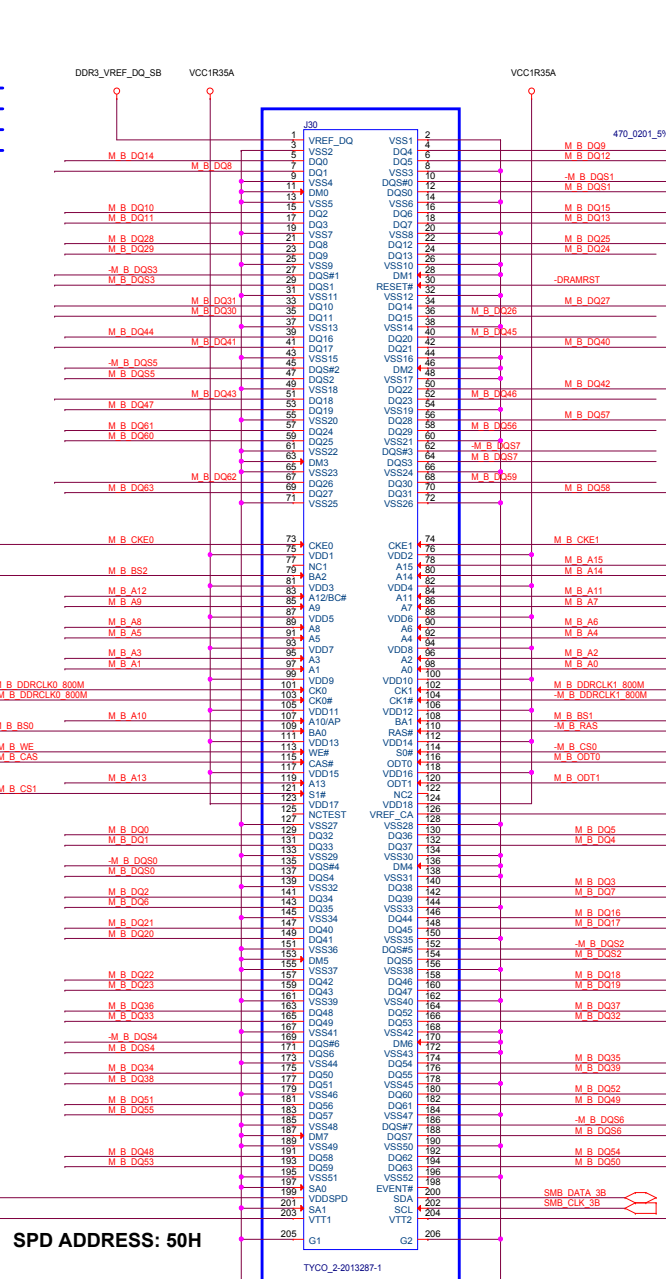
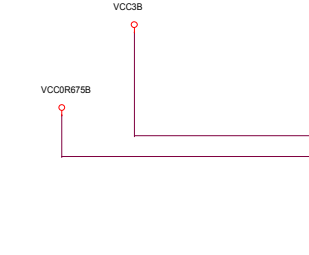
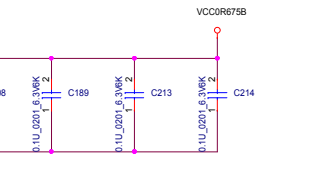


PLACE 1UF NEAR VCC1R35A PIN.

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<6> M_B_DQS[7:0]
<6> M_B_DQS[7:0]
<6> M_B_A[15:0]



<6> M_B_CKE0
<6> M_B_BS2
<6> M_B_BS0
<6> M_B_WE
<6> M_B_CAS
<6> M_B_CS1
<6> M_B_DDRCLK0_800M
<6> M_B_DDRCLK0_800M
<6> M_B_BS0
<6> M_B_WE
<6> M_B_CAS
<6> M_B_CS1




SPD ADDRESS: 50H


PLACE NEAR DIMM Slot

ST-1_SWG_SDV_EC173


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						<small>Challen</small>		<small>0.1</small>
						<small>Date:</small>	<small>Thursday, October 23, 2014</small>	<small>Sheet 32 of 100</small>


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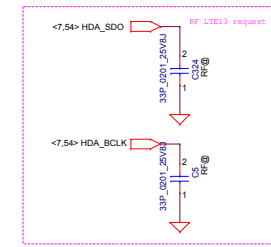
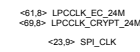
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						Date:	Thursday, October 23, 2014	Sheet 35 of 100

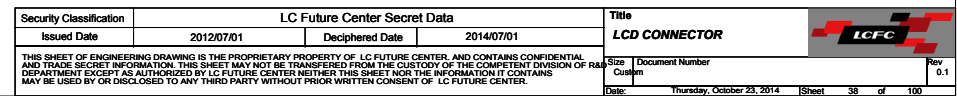
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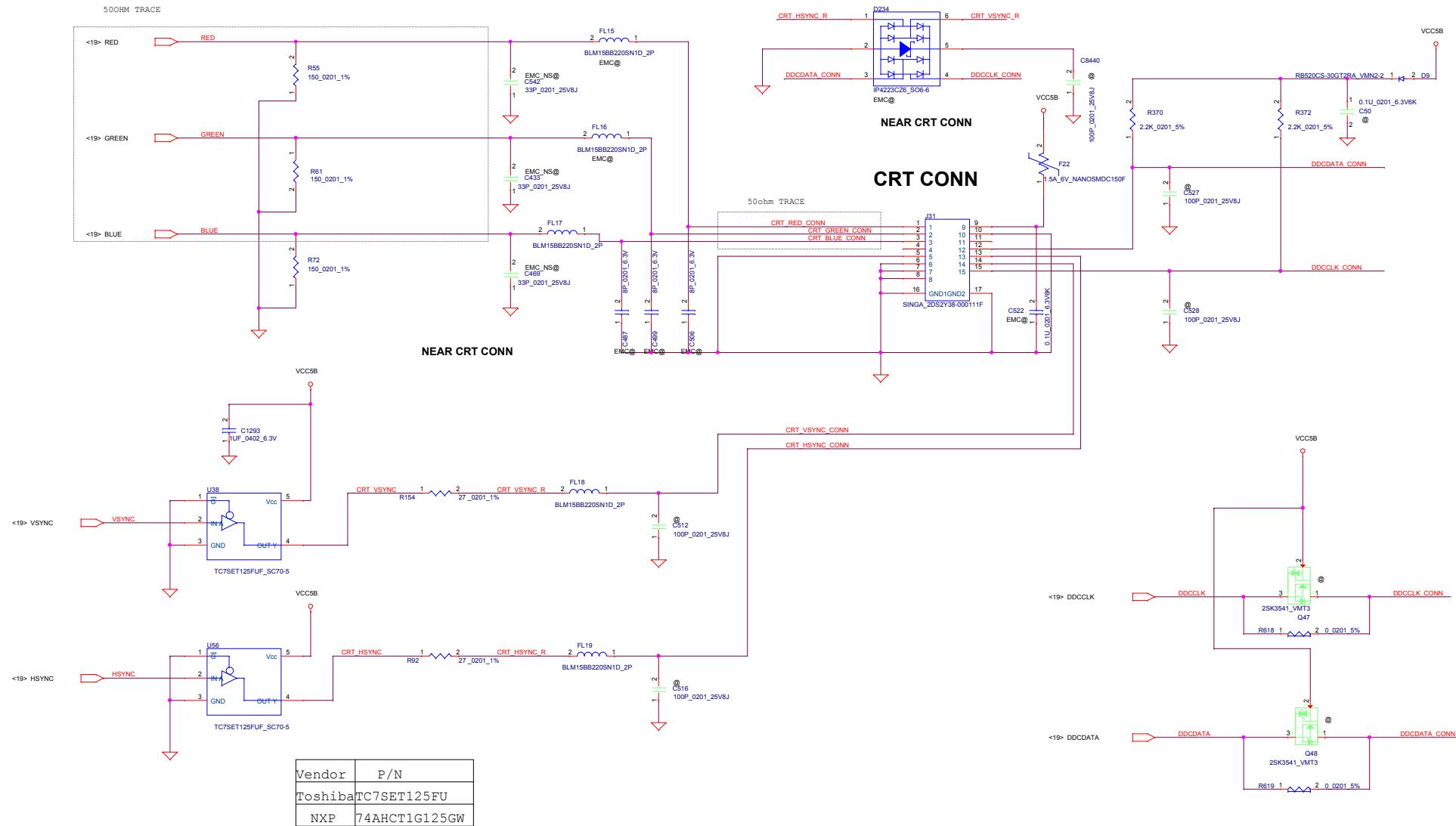


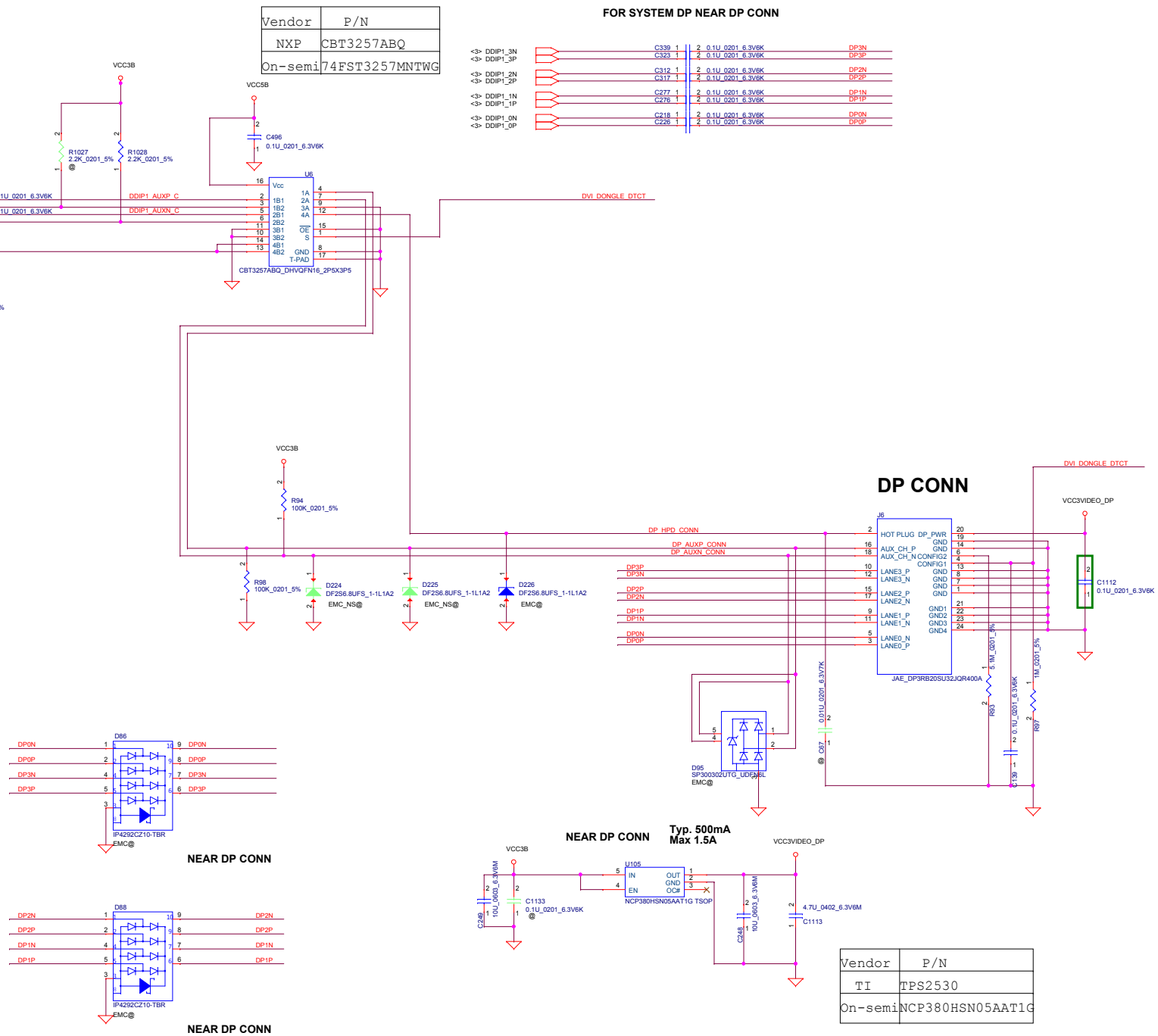
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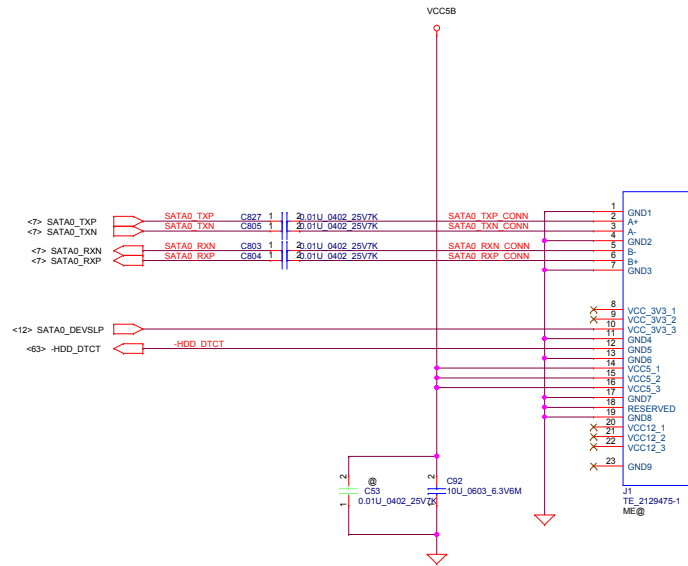
Vendor	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G

Security Classification	LC Future Center Secret Data			Title	DISPLAY PORT CONNECTOR			
Issued Date	2012/06/21	Deciphered Date	2012/06/21	Document Number	STING LUMA			
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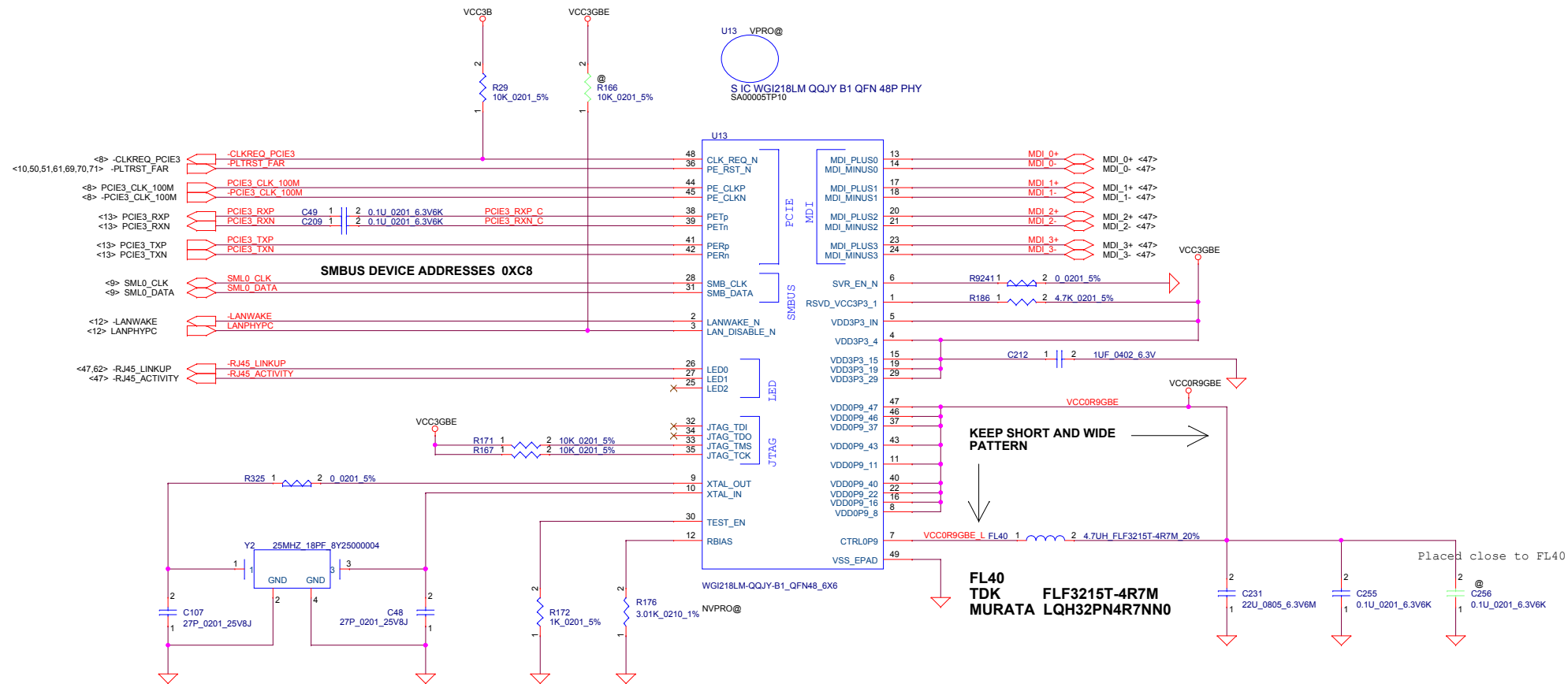
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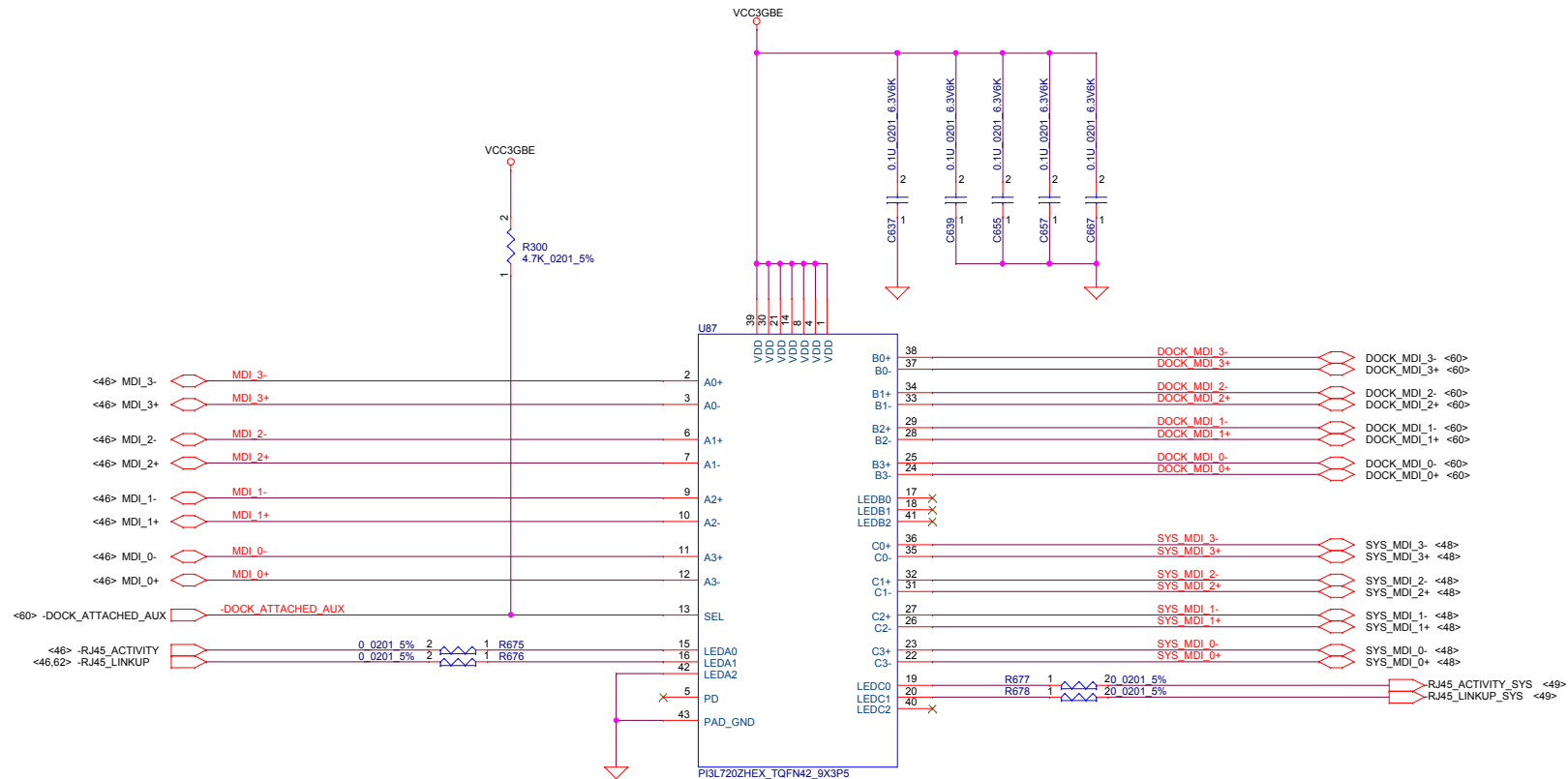
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TXC 8Y25000004
KDS 1ZZHAE25000CC0A
ESPON Q22FA1280023800

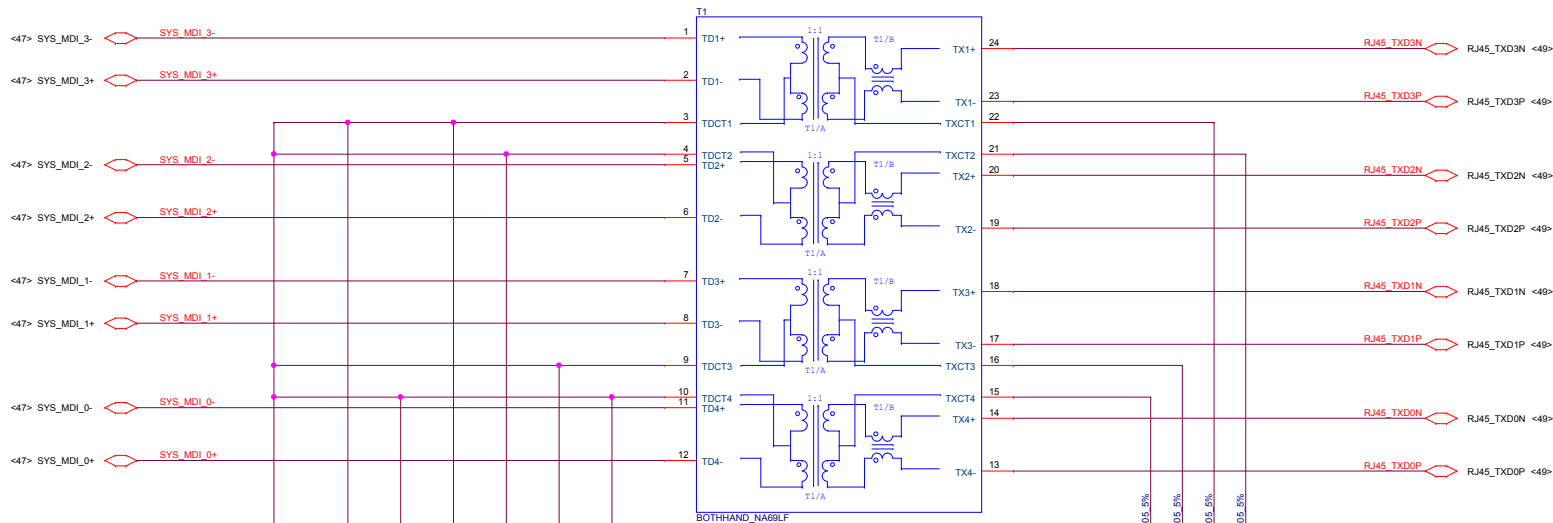
U13 GBE PHY

vPRO Model	Non-vPRO Model
I218LM	I218V



U87

Vendor	P/N
Pericom ST micro Onsemi	PI3L720ZHE STMUX1800E NCN7201



THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

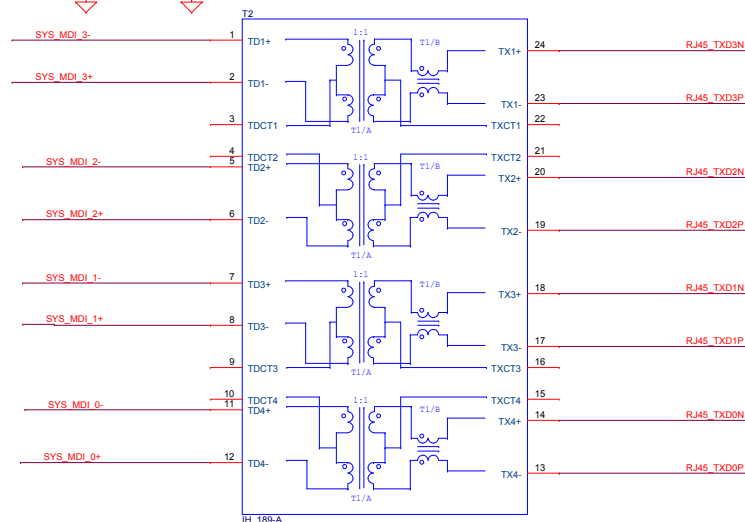
C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

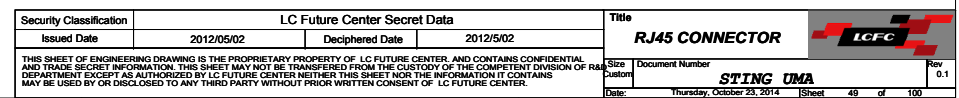
ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothhand	NA69LF

PATTERN MUST BE SHORT AND WIDE.

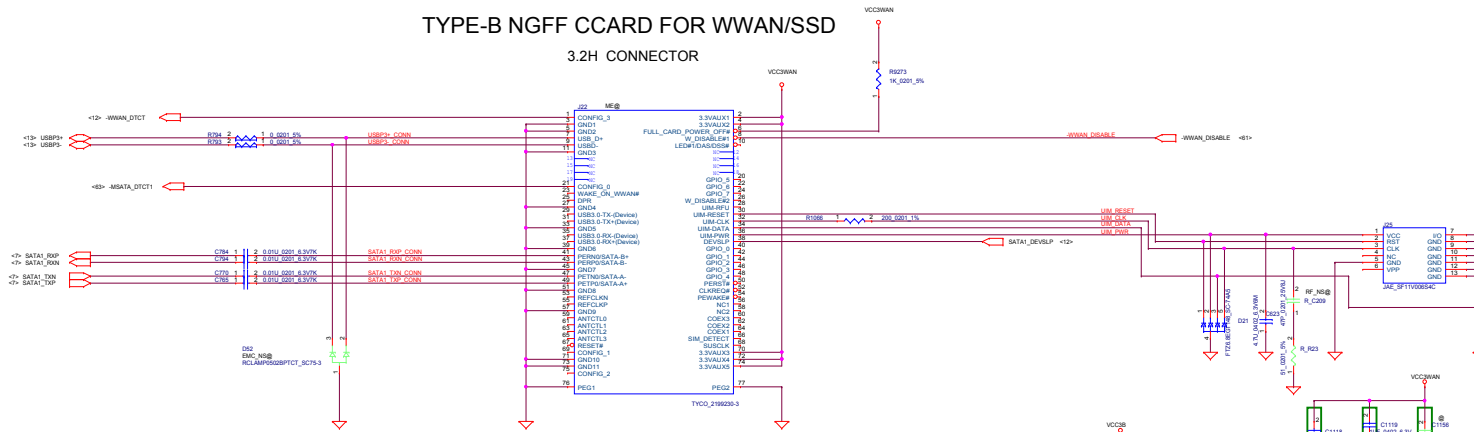
HIGH VOLTAGE
1500PF CAP
IS OPTIONAL





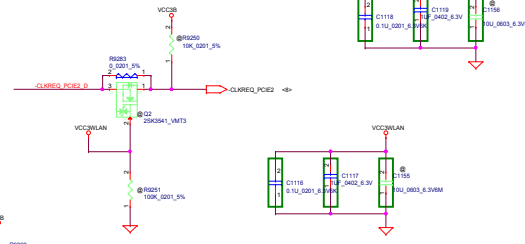
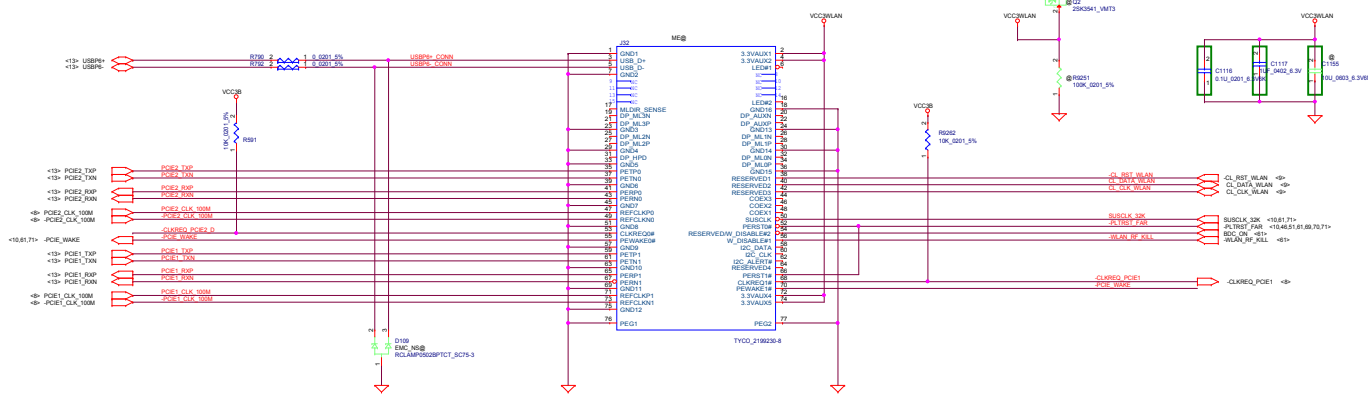
TYPE-B NGFF CCARD FOR WWAN/SSD

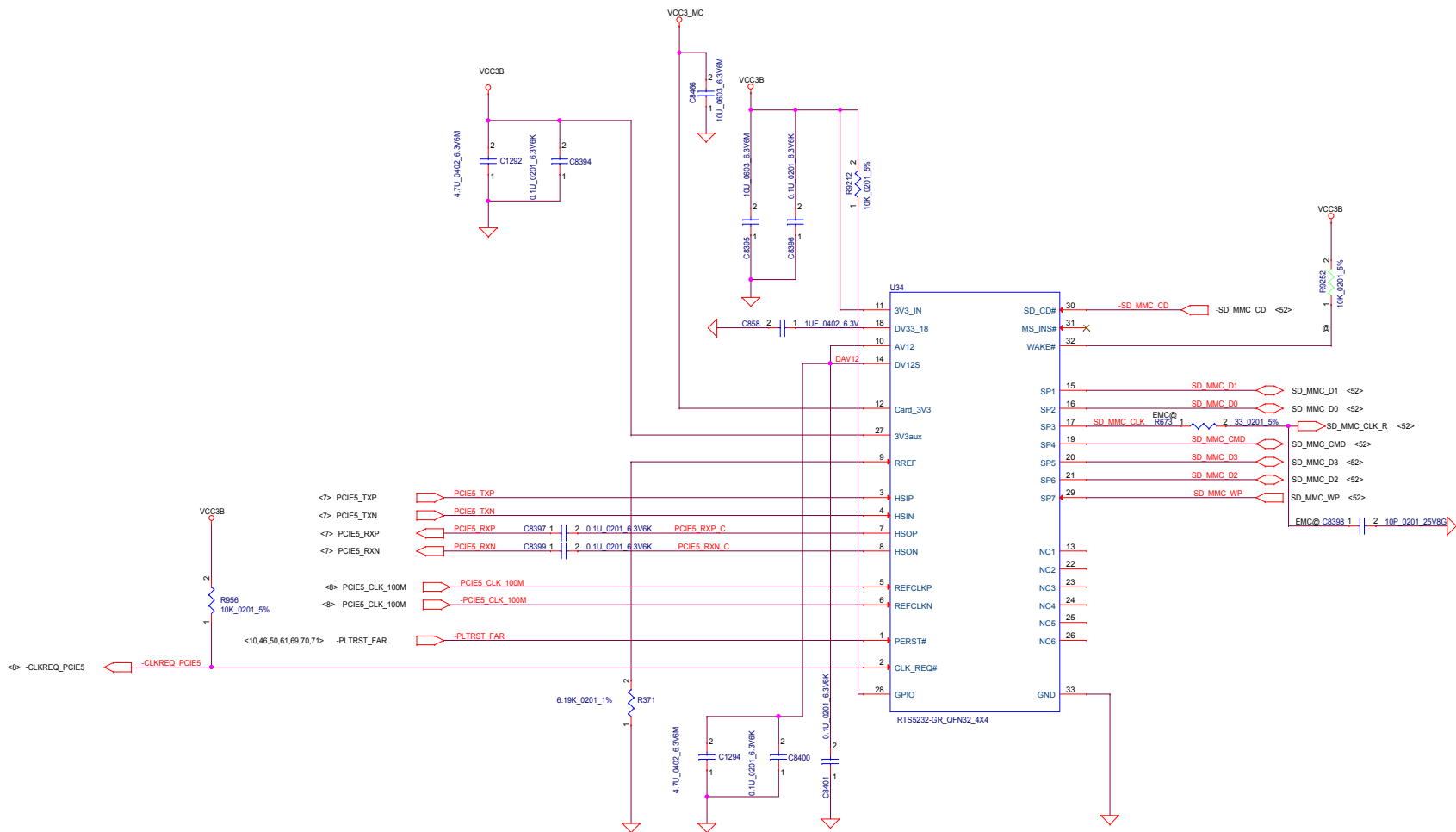
3.2H CONNECTOR

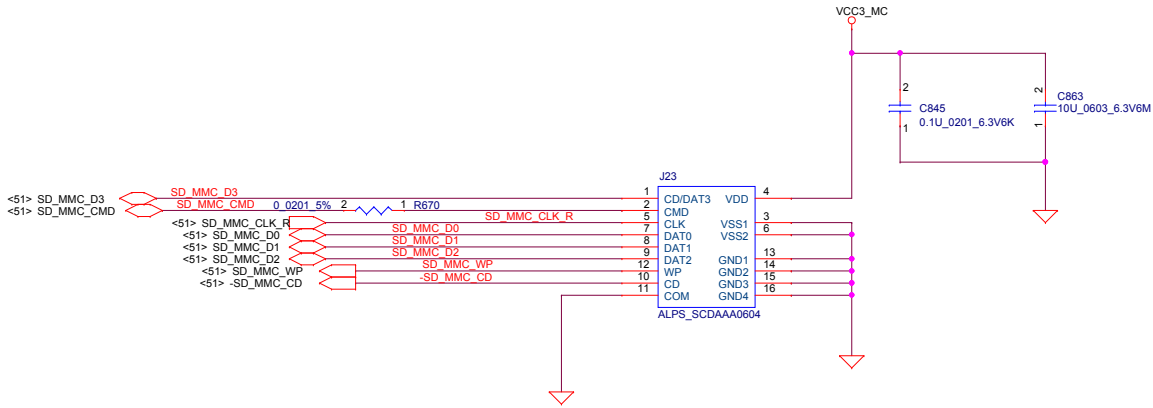


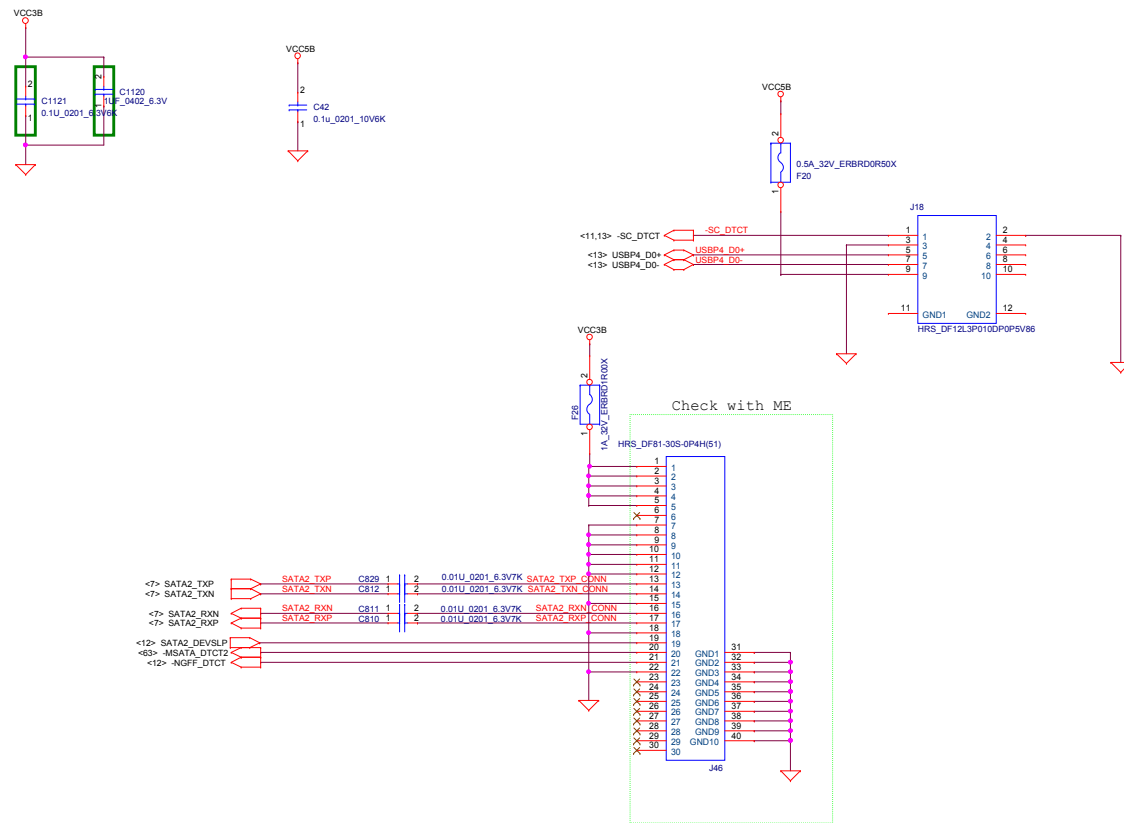
TYPE-A NGFF CCARD FOR WLAN

3.2H CONNECTOR









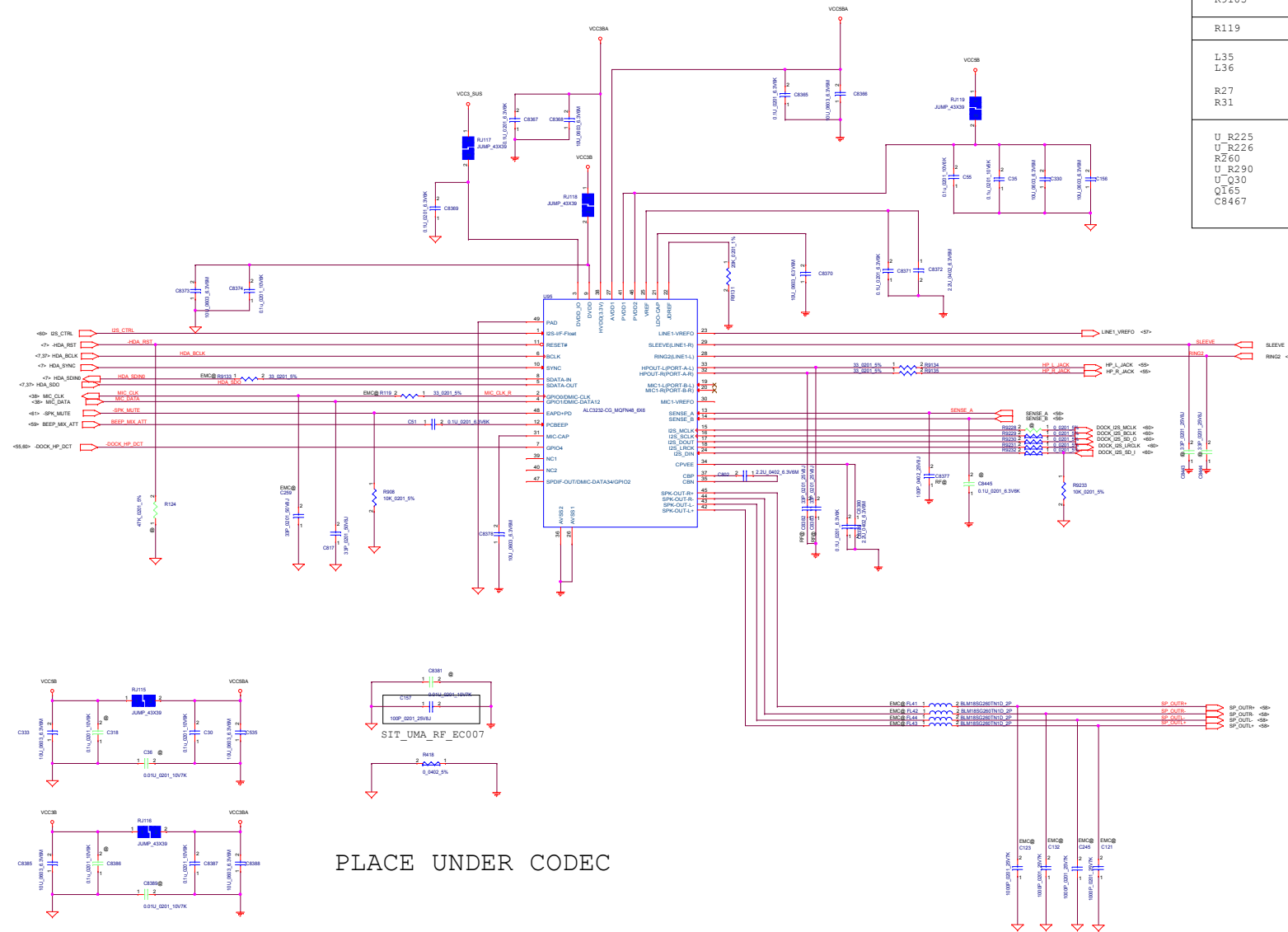
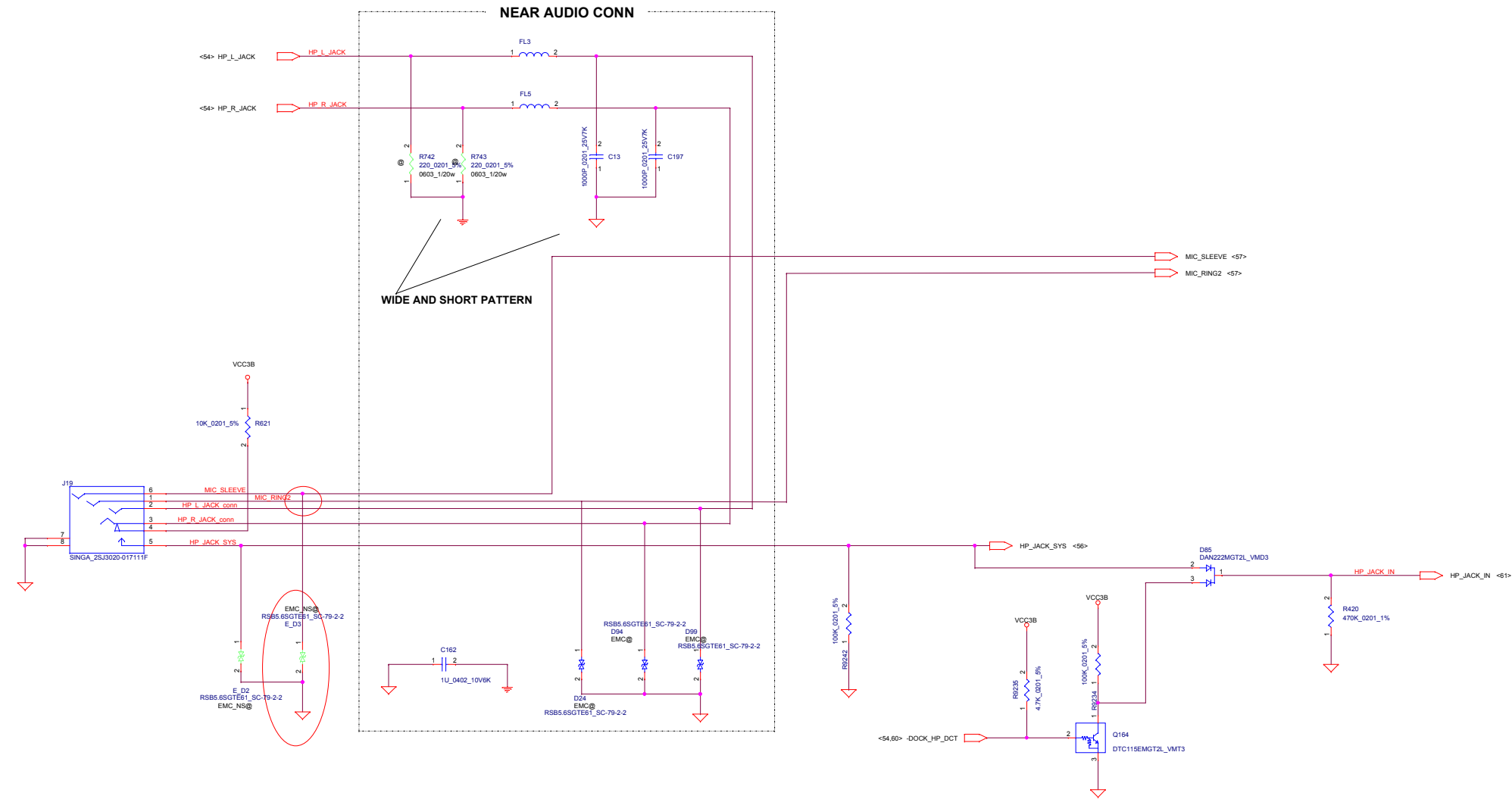


Table MIC HW Enable/Disable		
	Enable	Disable
R9097 R9105	No ASM ASM	ASM No ASM
R119	ASM	No ASM
L35 L36	ASM ASM	No ASM No ASM
R27 R31	No ASM No ASM	ASM ASM
U R225 U R226 RZ60 U R290 U Q30 Q165 C8467	ASM ASM ASM ASM ASM ASM ASM	No ASM No ASM No ASM No ASM No ASM No ASM No ASM

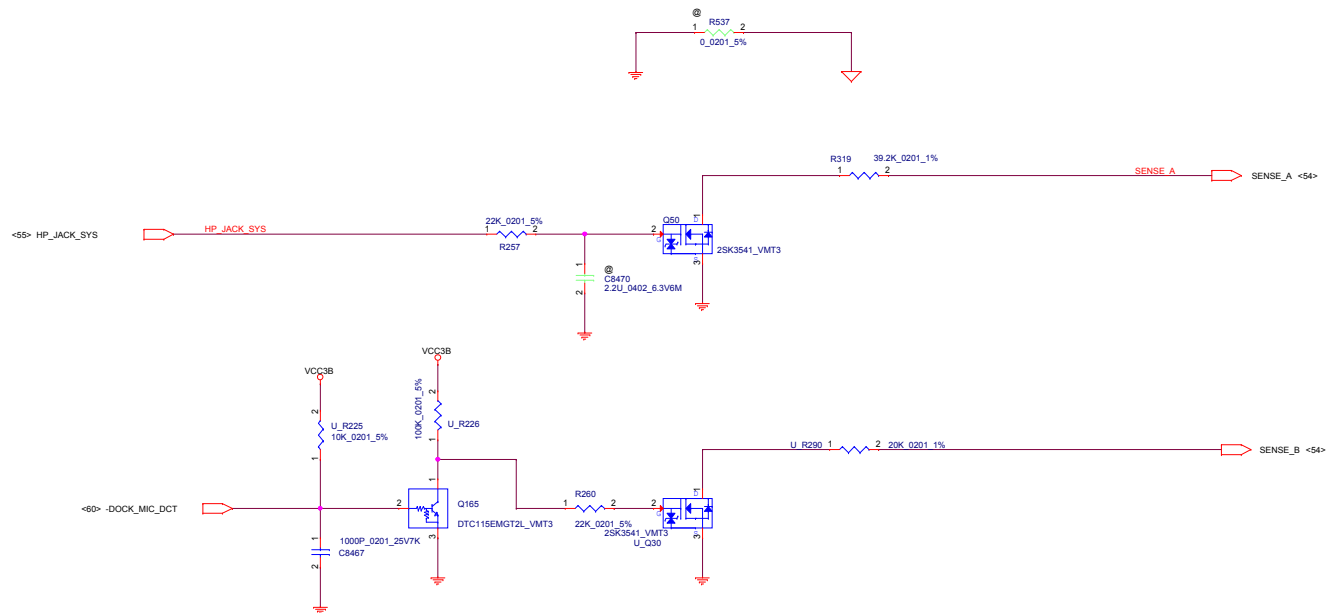
LOGIC

PLACE UNDER CODEC

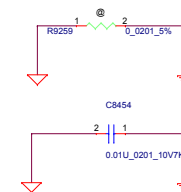
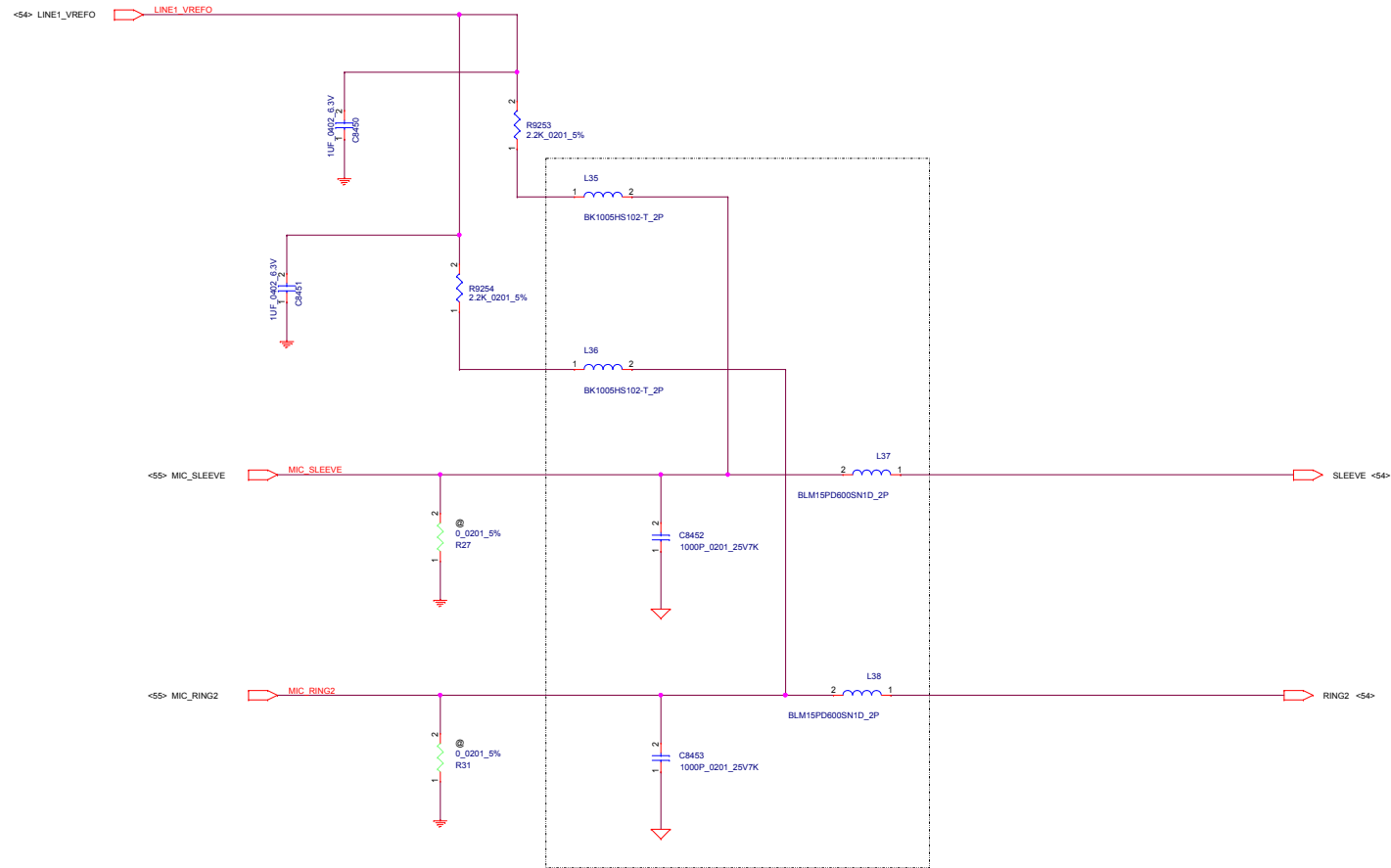


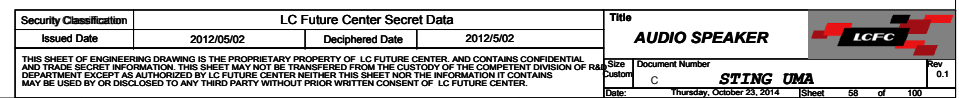
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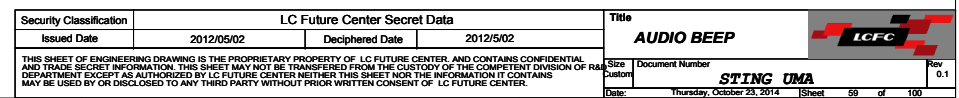


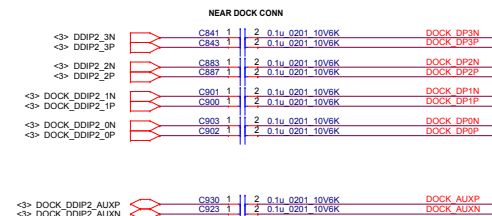
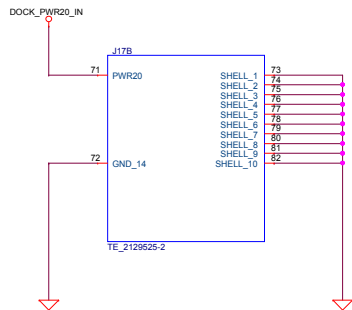
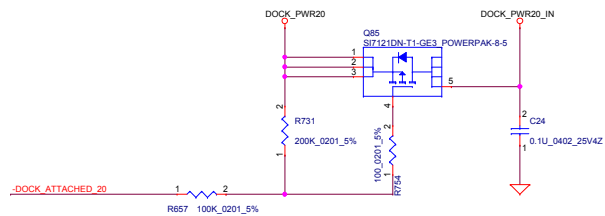
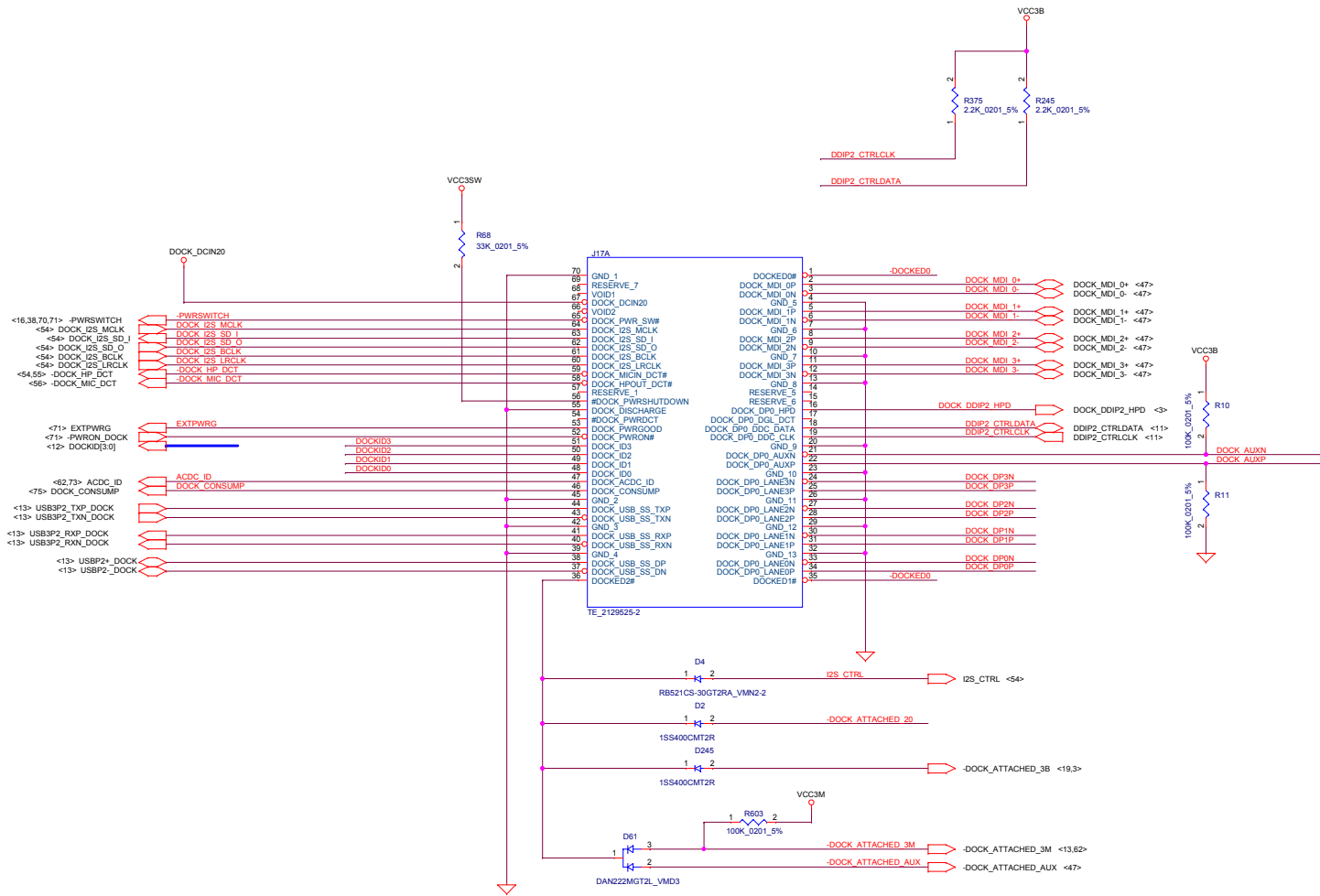


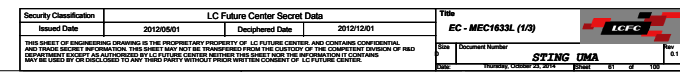
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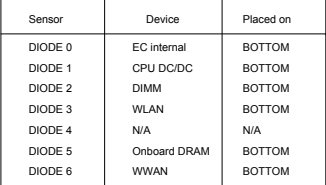


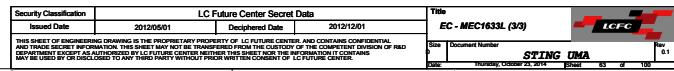


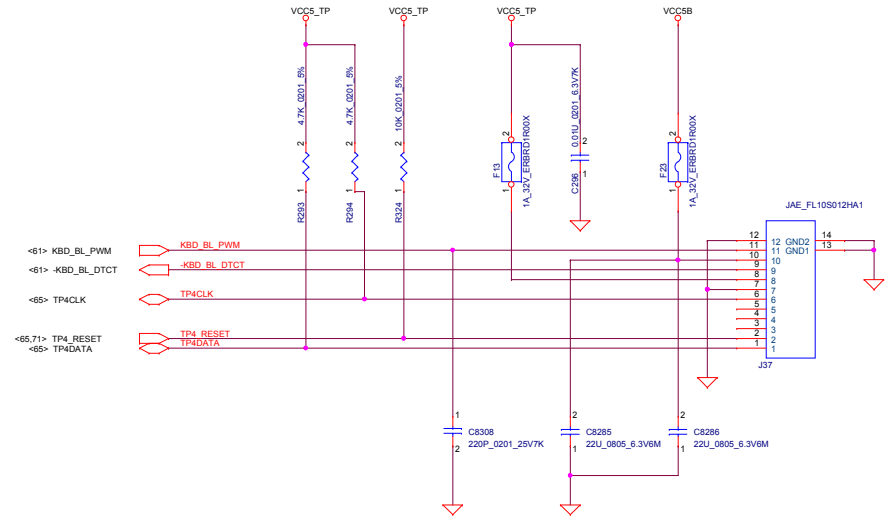
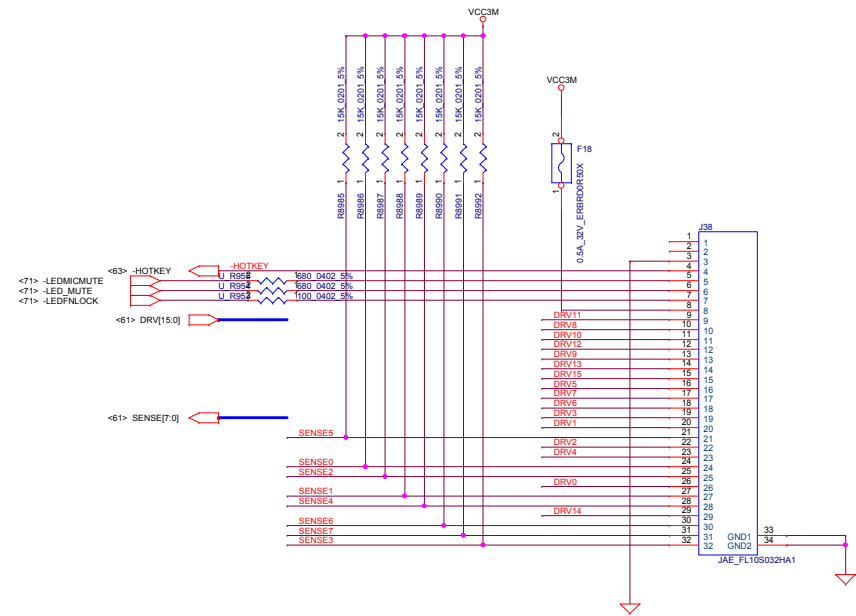




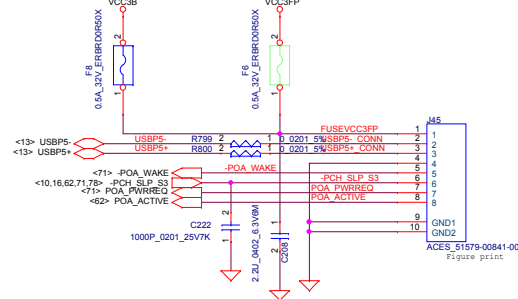
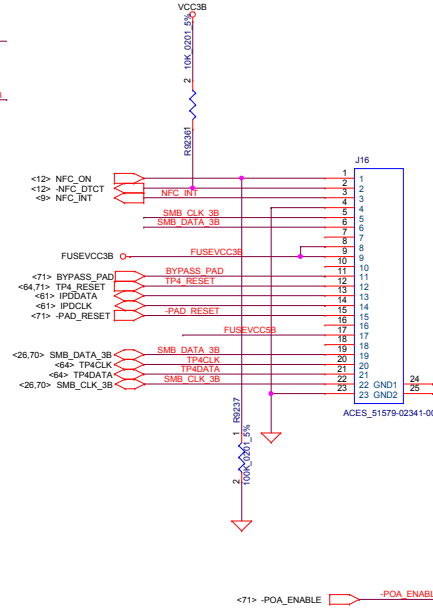
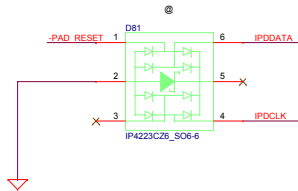
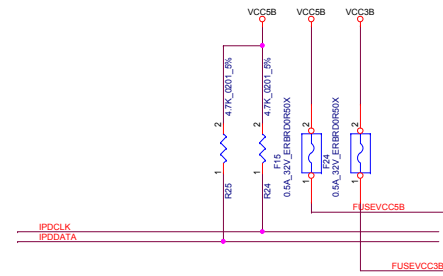




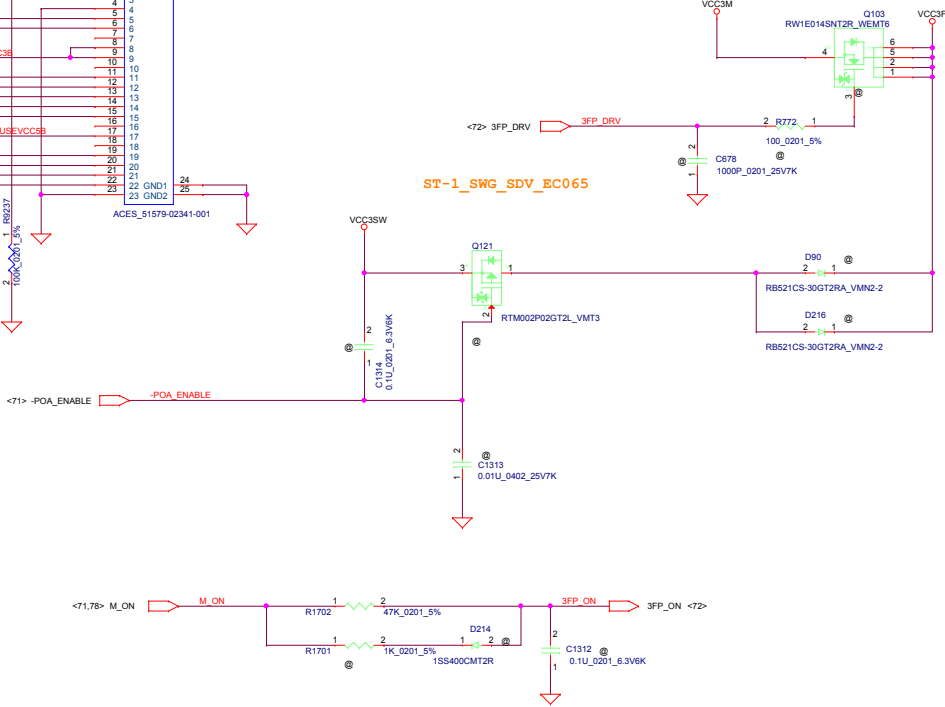





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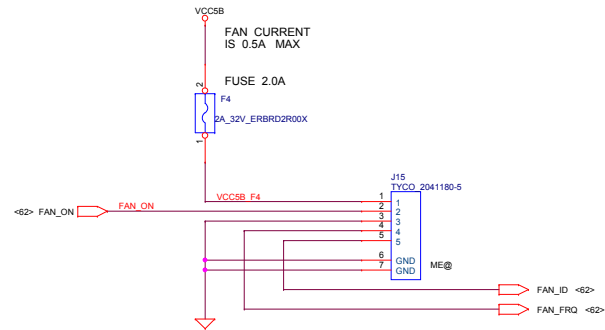


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						Date:	Thursday, October 23, 2014	Sheet 66 of 100




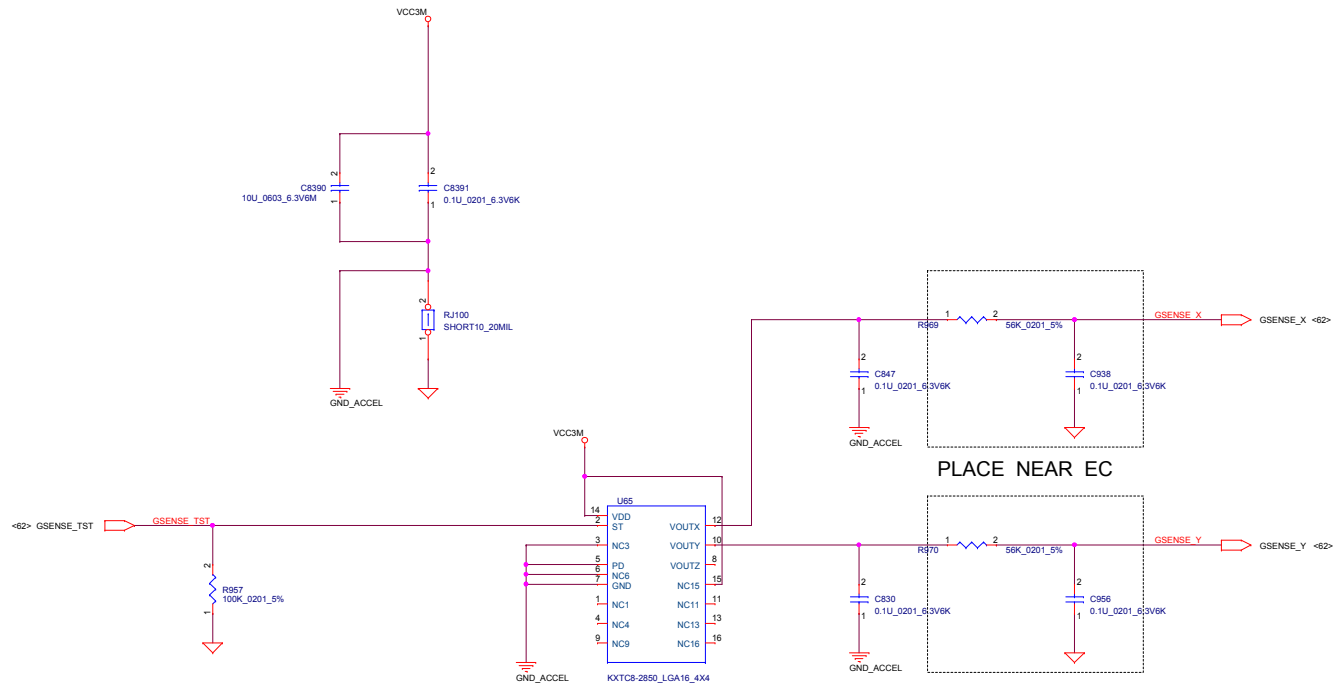
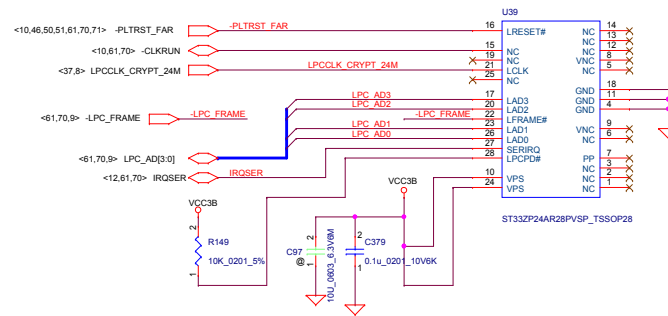
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					STING UMA	0.1
				Date:	Thursday, October 23, 2014	Sheet 67 of 100

TABLE		
	LIS34AL KXTC8-2850	NO ACC.
R401 R957	NO_ASM ASM	ASM ASM
U65	ASM	NO_ASM
Q105	ASM	NO_ASM
R885 C829 C969	10-OHM ASM ASM	NO_ASM NO_ASM NO_ASM
C830 C847	ASM ASM	NO_ASM NO_ASM
R969 C938 R970 C956	56K ASM 56K ASM	NO_ASM NO_ASM NO_ASM NO_ASM
C704 C944 C703	NO_ASM NO_ASM NO_ASM	NO_ASM NO_ASM NO_ASM
R125	ASM	ASM





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				Sheet	69 of 100
				Rev	0.1

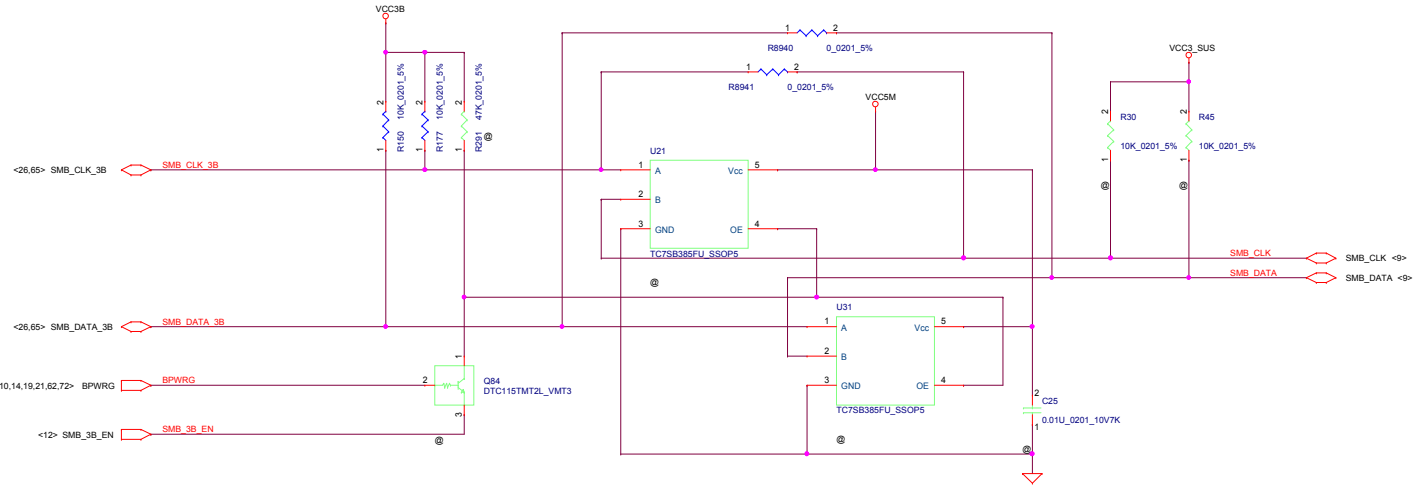
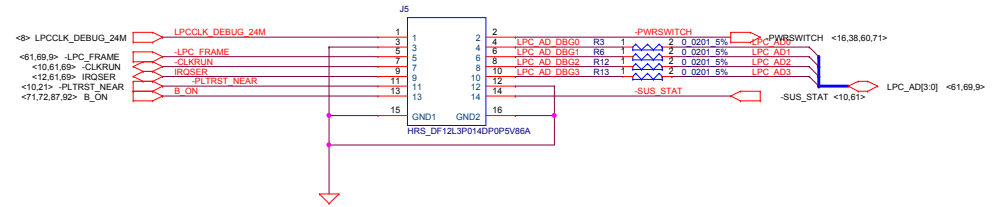
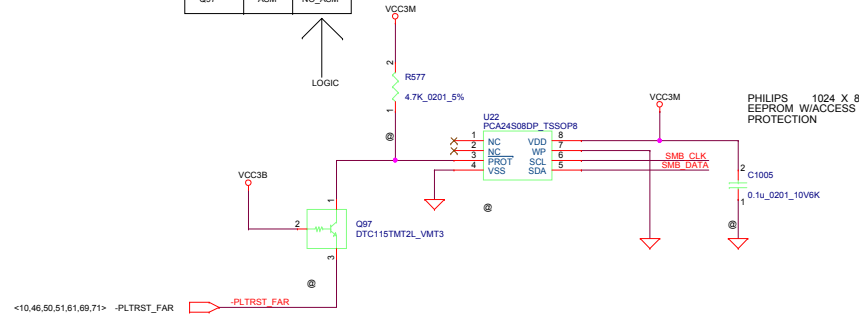
TABLE

EEPROM	U22	U23
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C1005	ASM	NO_ASM
R577	ASM	NO_ASM
Q97	ASM	NO_ASM

LOGIC

LPC Debug Port

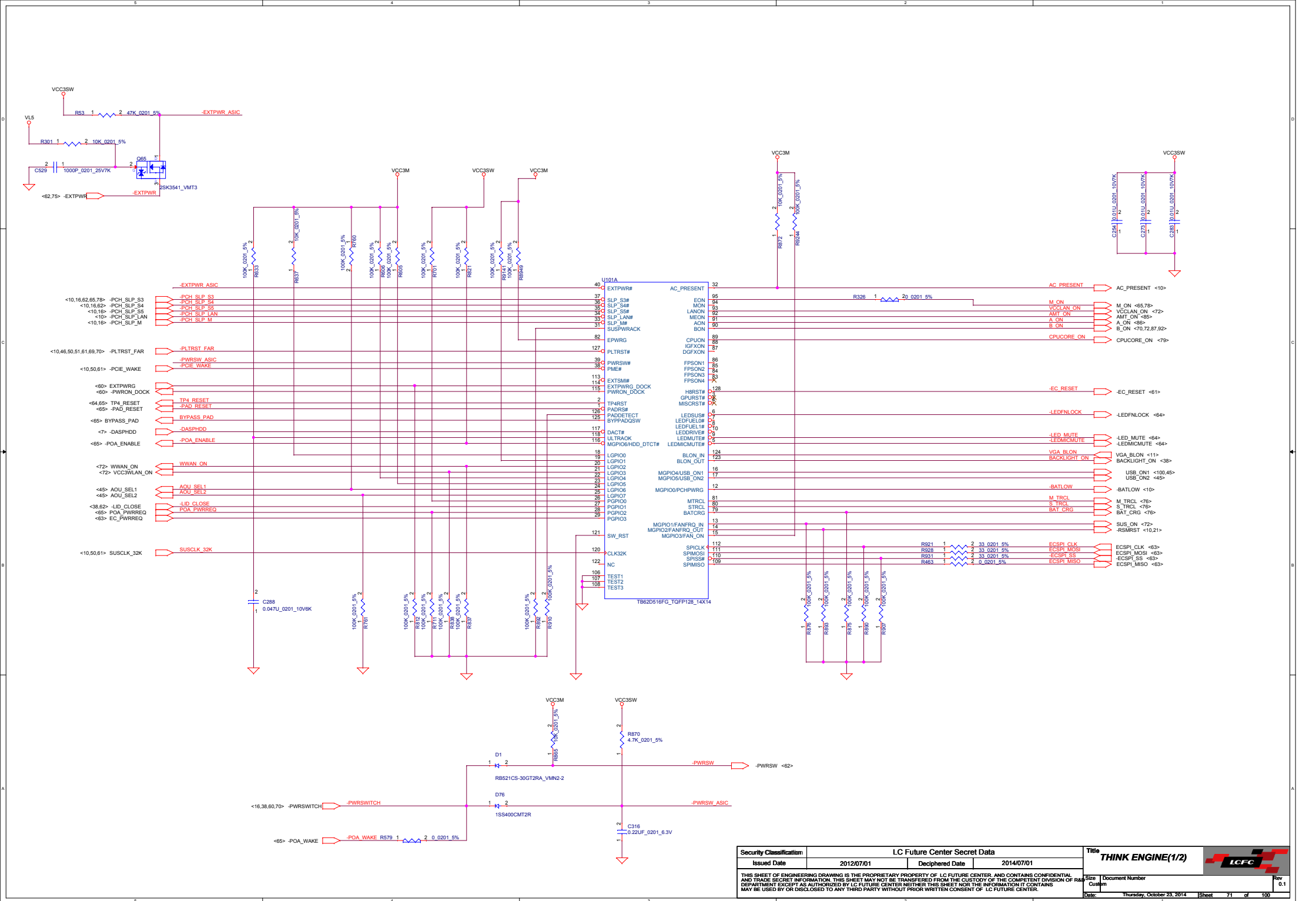
	Planar Only	BOX
J5	ASM	NO_ASM
R9062	ASM	ASM



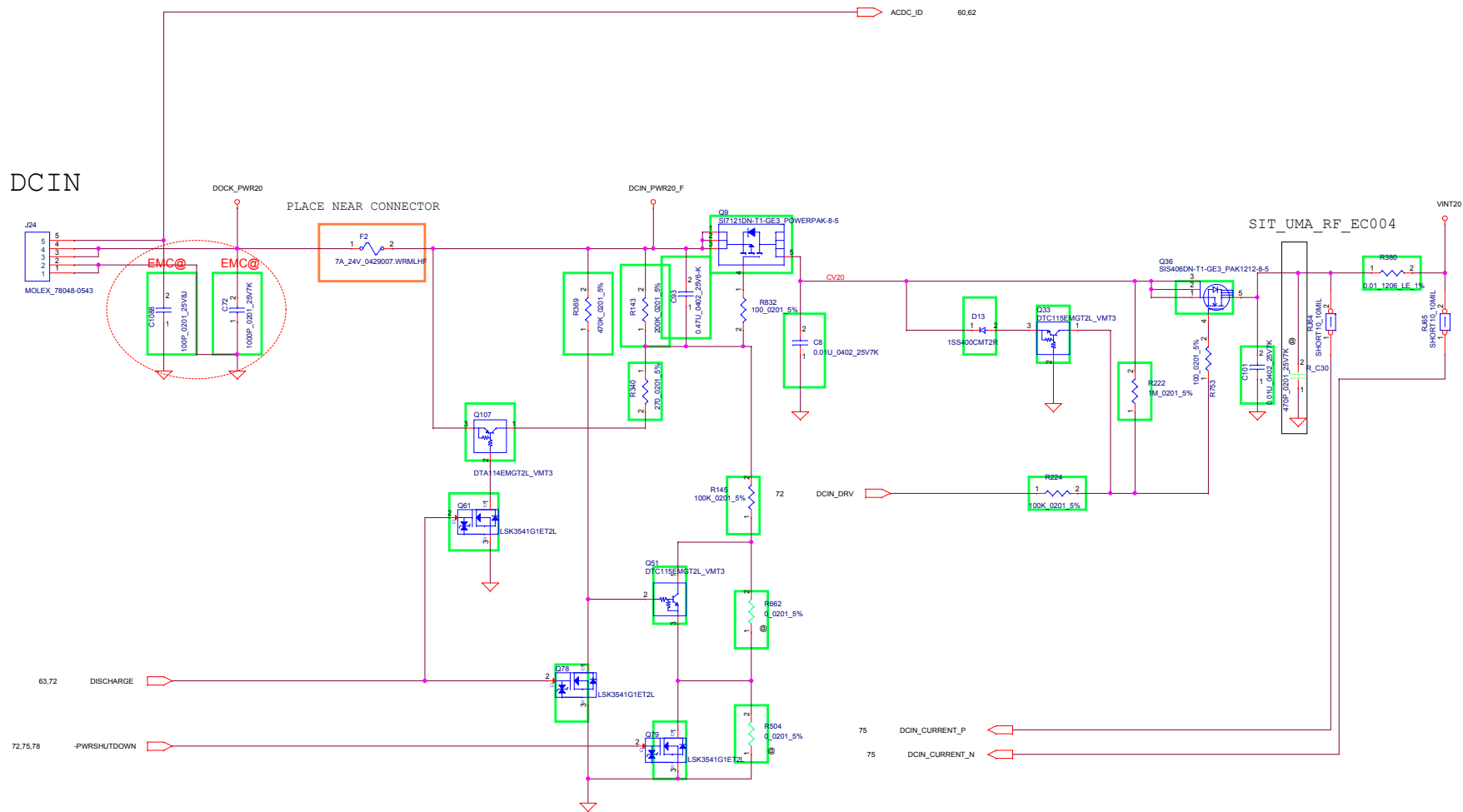
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U21	ASM	NO_ASM
U31	ASM	NO_ASM
C25	ASM	NO_ASM
R291	ASM	NO_ASM
Q84	ASM	NO_ASM
R8941	NO_ASM	ASM
R8940	NO_ASM	ASM
R30	ASM	NO_ASM
R45	ASM	NO_ASM

LOGIC



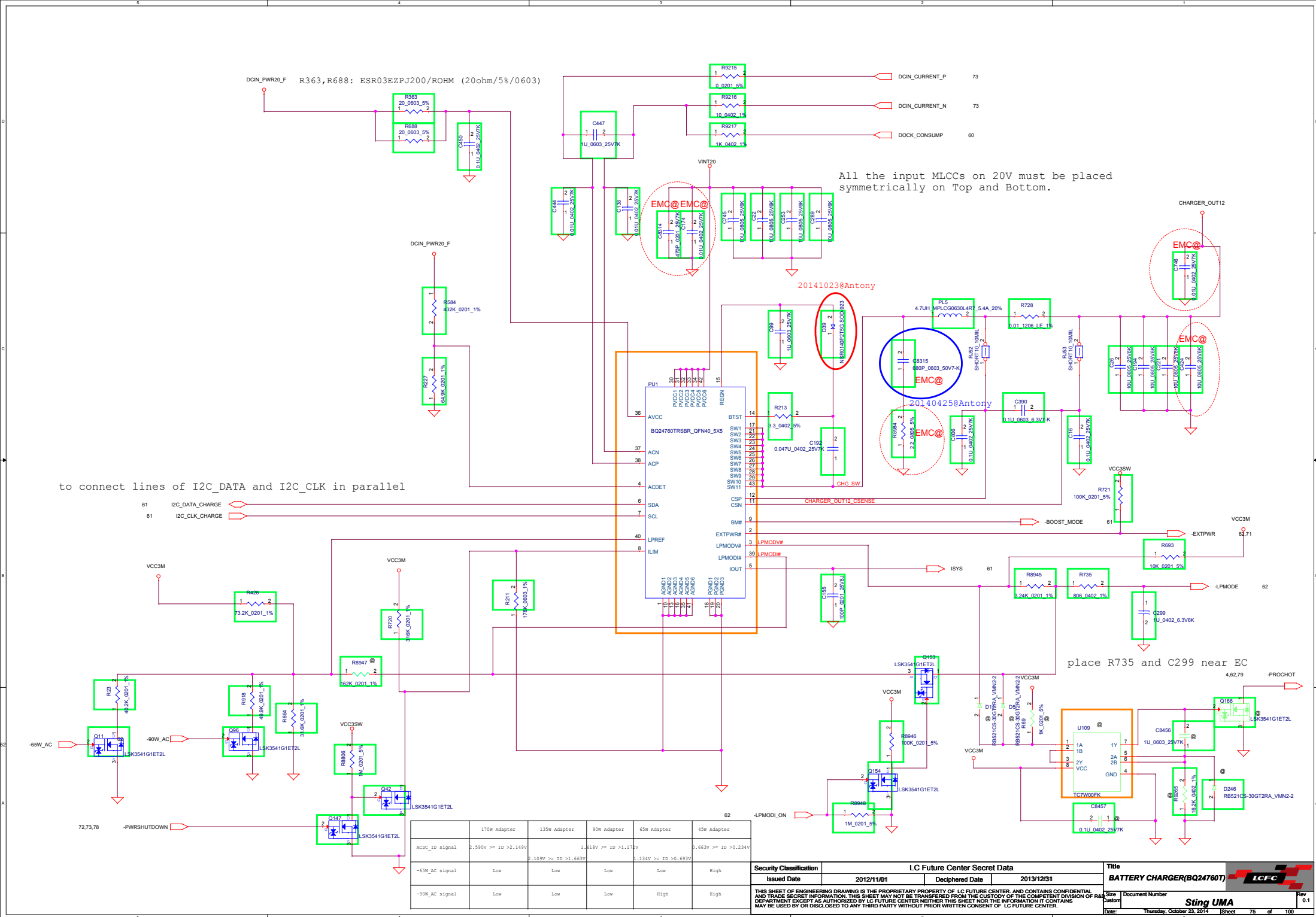
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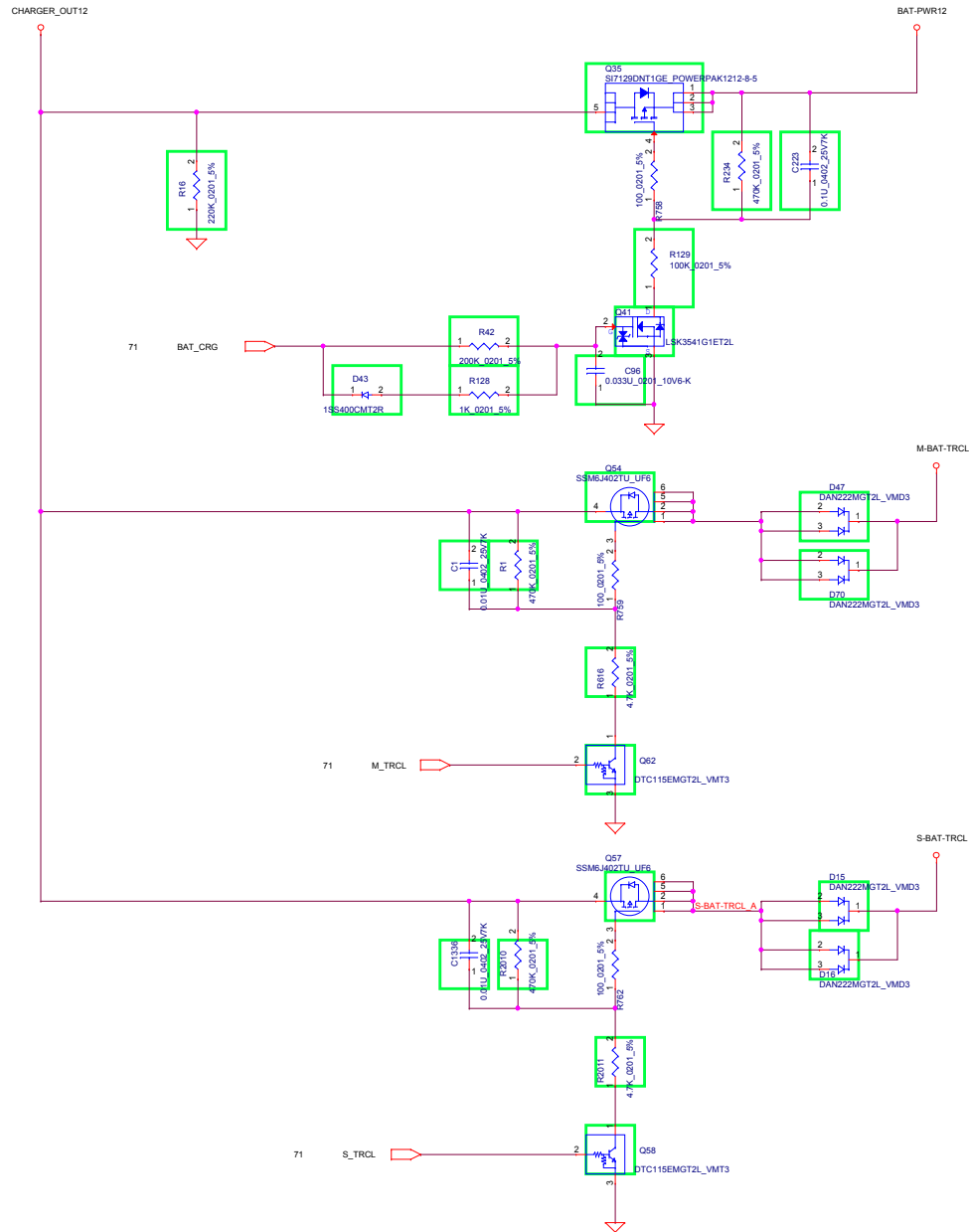


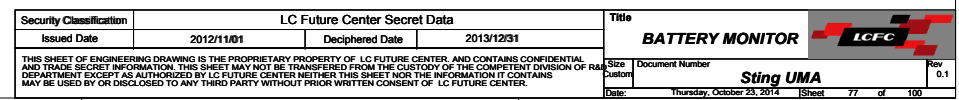
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R662	NO-ASM	ASM
R369	ASM	NO-ASM
Q78	ASM	NO-ASM
Q51	ASM	NO-ASM

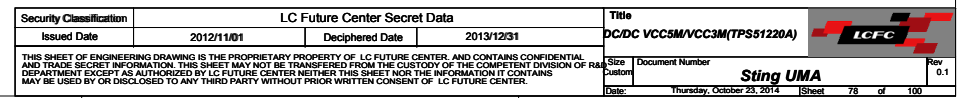
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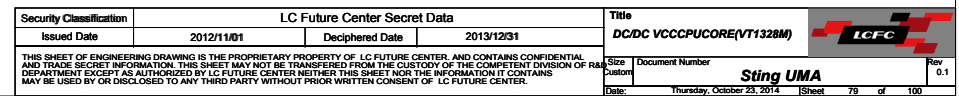


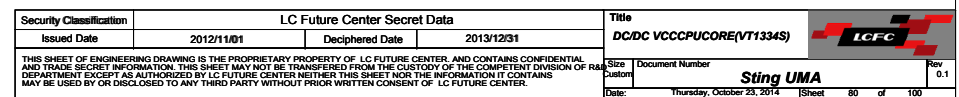





All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

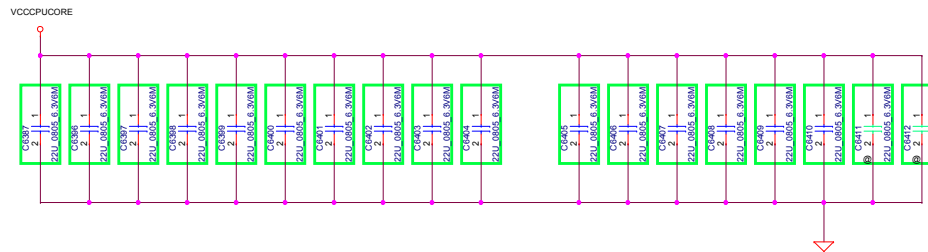







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16pcs 22uF for VCCCPUCORE of 25W ULT CPU
(14pcs 22uF for VCCCPUCORE of 15W ULT CPU)

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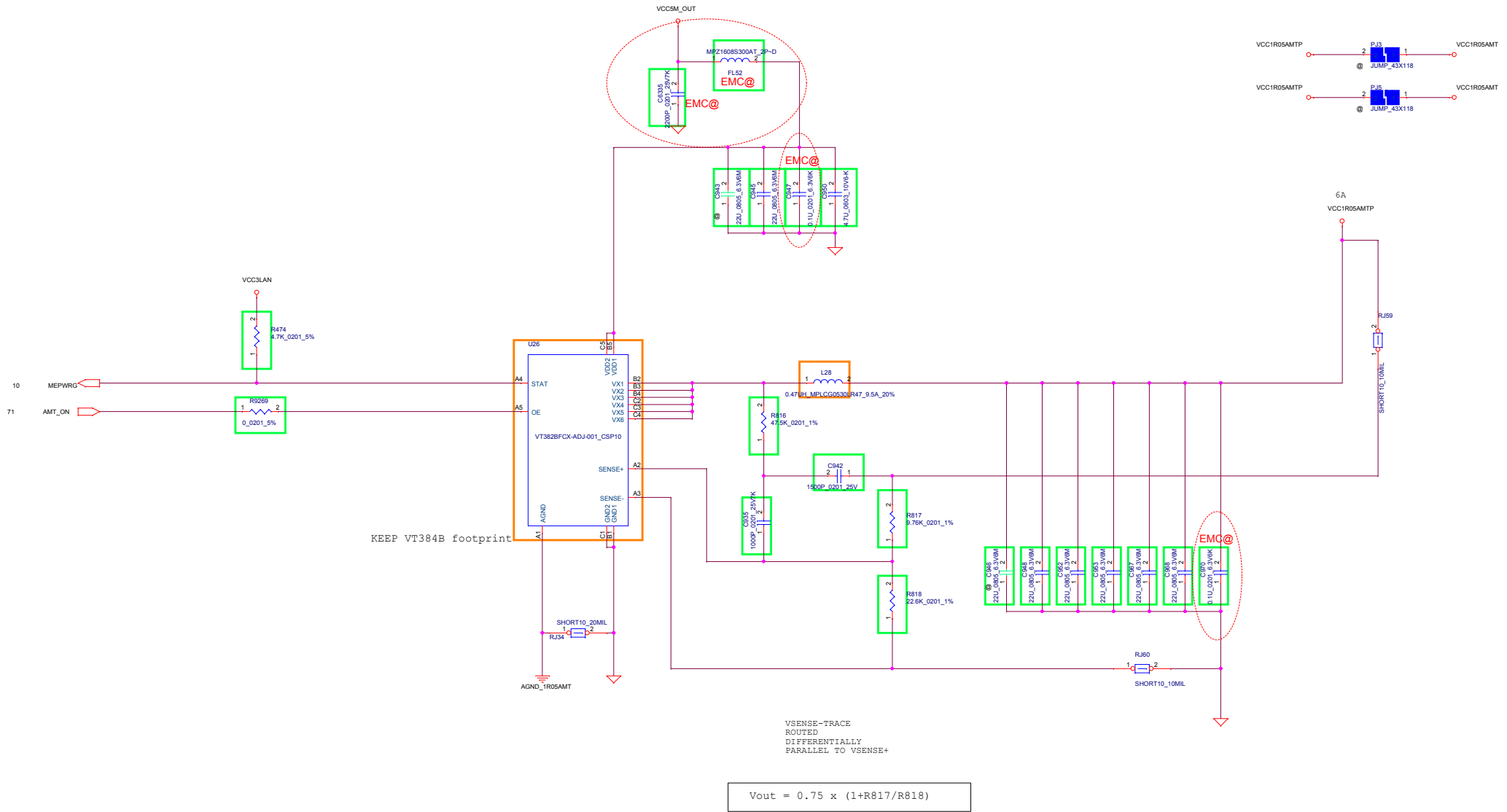
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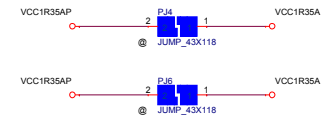
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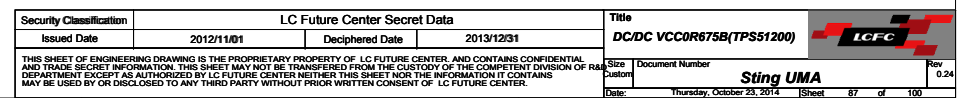
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VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+


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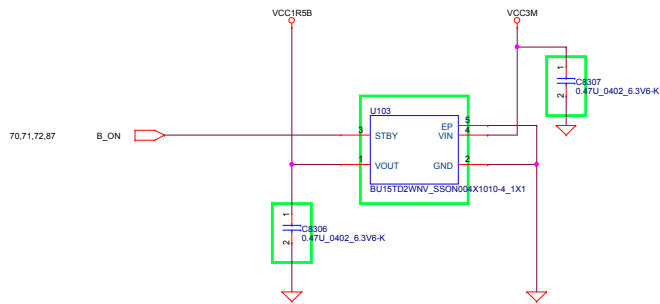
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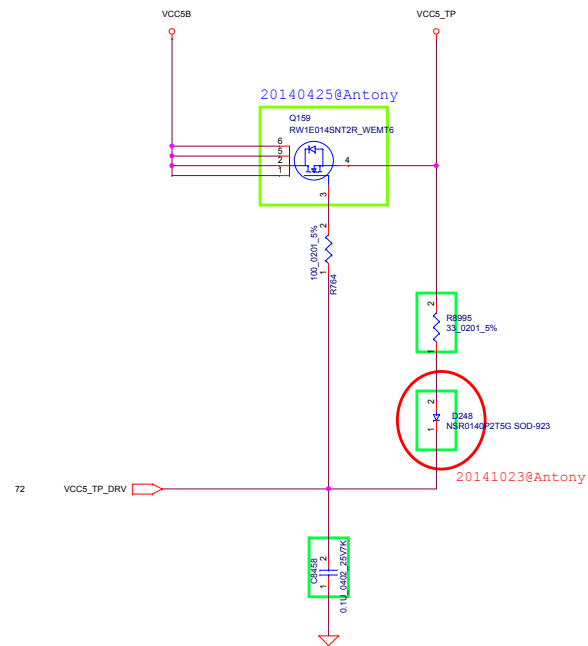
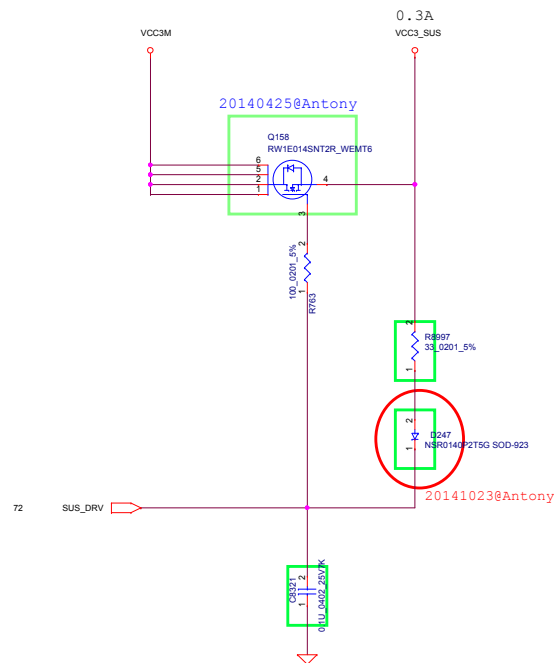
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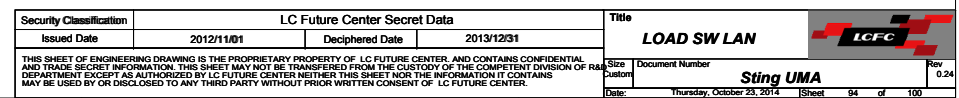
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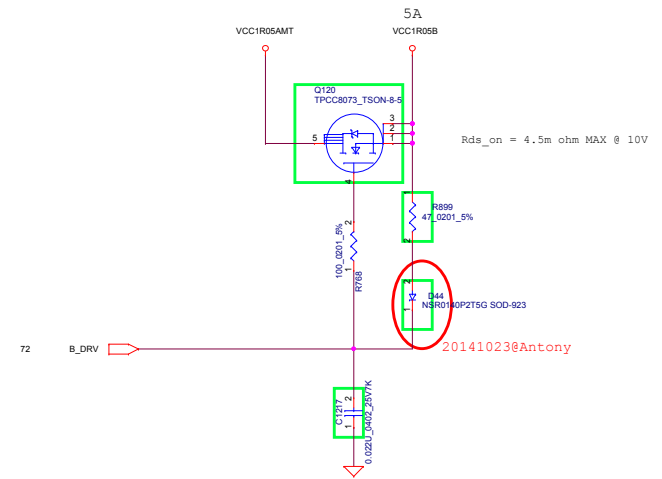
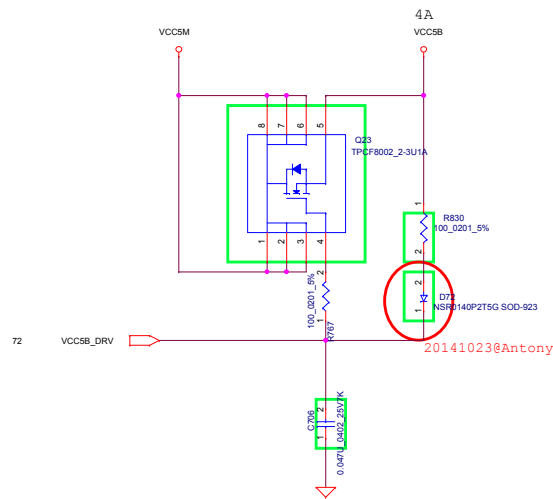
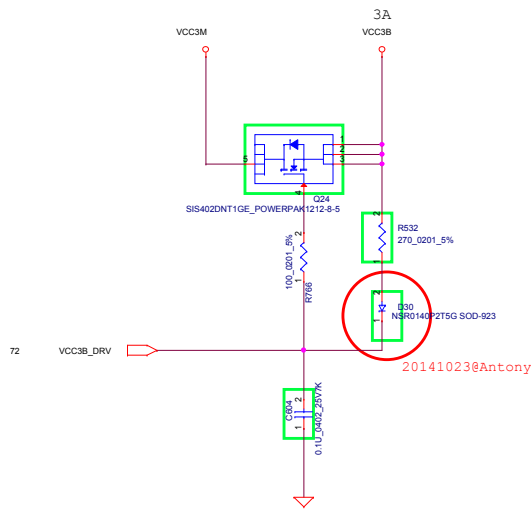


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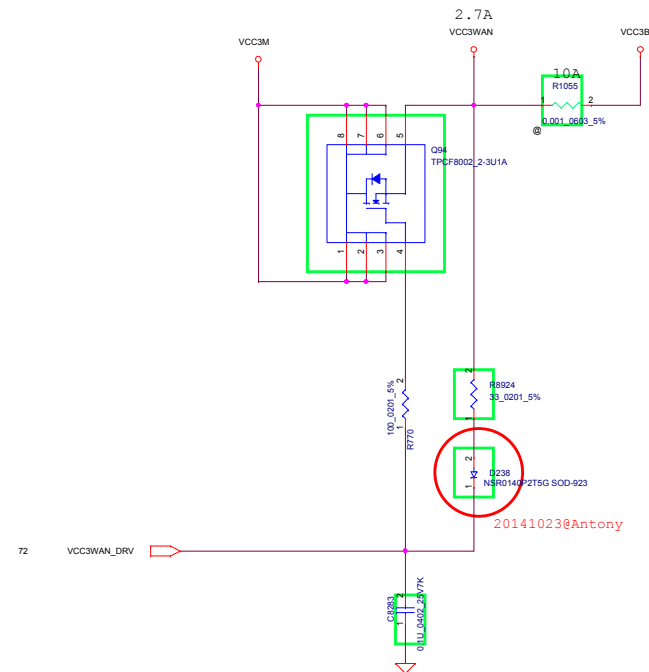
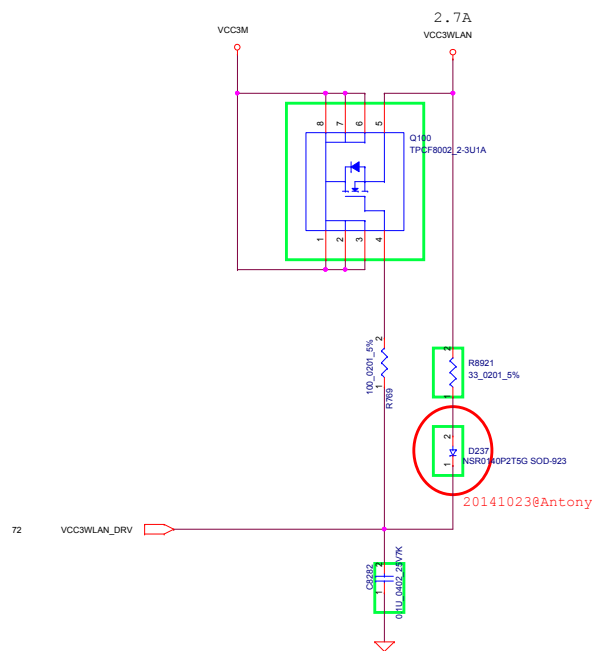
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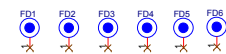
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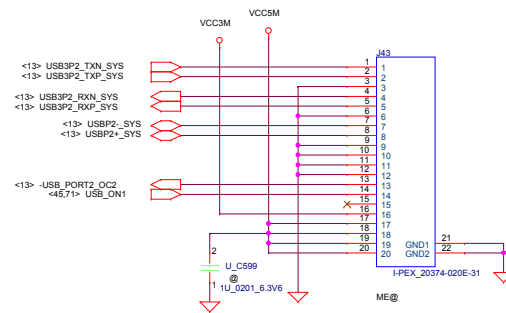



TABLE

AOAC	YES	NO
R1055	NO-ASM	ASM
Q94	ASM	NO-ASM
R8924	ASM	NO-ASM
R8926	ASM	NO-ASM
C8283	ASM	NO-ASM
D238	ASM	NO-ASM

↑
LOGIC





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